19-3376; Rev 1; 1/05

Quad SPST, High-Bandwidth, Signal Line Protection Switch

General Description

The MAX4854H/MAX4854HL analog switches operate from a single +2V to +5.5V supply and can handle signals greater than the supply rail. These devices feature four low on-resistance (7Ω) single-pole/single-throw (SPST) switches, with 27.5pF on-capacitance, making them ideal for data signals. If the input signal exceeds the supply rail, the switches become high impedance and prevent the signal from feeding through to the output.

The MAX4854H/MAX4854HL are available in the space-saving (3mm x 3mm), 16-pin, thin QFN package and operate over the extended (-40°C to +85°C) temperature range.

Applications

USB Switching

High-Bandwidth Data Switching

Cellular Phones

Notebook Computers

PDAs and Other Handheld Devices

Features

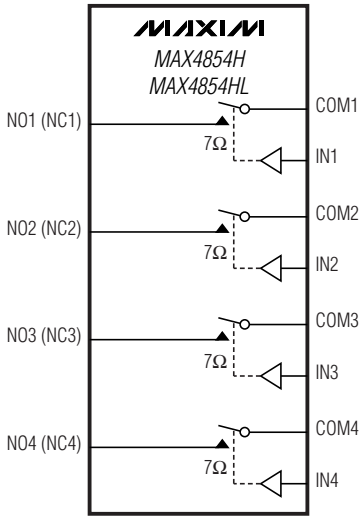
- **USB 2.0 Full Speed (12MB) and USB 1.1 Signal Switching**
- **Overvoltage Protection if Signal Exceeds V_{CC}**
- **150MHz -3dB Bandwidth**
- **27.5pF On-Capacitance**
- **+2V to +5.5V Supply Range**
- **7Ω On-Resistance**
- **Low 10µA Supply Current**
- **1.8V Logic Compatible**
- **Available in a Space-Saving (3mm x 3mm) 16-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4854HETE	-40°C to +85°C	16 TQFN-EP*	ACD
MAX4854HLETE	-40°C to +85°C	16 TQFN-EP*	ACX

**EP = Exposed paddle.*

Block Diagram/Truth Table



MAX4854H	
IN_	NO_
0	OFF
1	ON

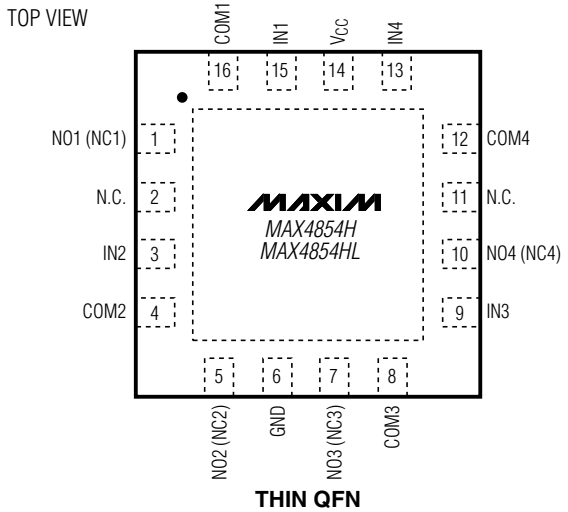
SWITCHES SHOWN FOR LOGIC 0 INPUT

MAX4854HL	
IN_	NC_
0	ON
1	OFF

SWITCHES SHOWN FOR LOGIC 1 INPUT

( ) INDICATES THE MAX4854HL

Pin Configuration



CONNECT EXPOSED PADDLE TO PC BOARD GROUND.
( ) INDICATES THE MAX4854HL

Quad SPST, High-Bandwidth, Signal Line Protection Switch

ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN_, COM_, NO_, NC_ to GND (Note 1) .....-0.3V to +6.0V
Closed Switch Continuous Current COM_, NO_, NC_ .....±50mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 50% duty cycle) .....±100mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle) .....±120mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NO_/NC_ or COM_ exceeding GND are clamped by internal diodes. Signals on IN exceeding GND are clamped by an internal diode. Limit the forward-diode current to the maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}			2.0		5.5	V
Supply Current	I_{CC}	V_{CC} = 5.5V, $V_{IN\_}$ = 0V or V_{CC}			10	20	µA
ANALOG SWITCH							
Analog Signal Range	$V_{NO\_}$, $V_{COM\_}$			0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 3V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V_{CC}	T_A = +25°C		7	9	Ω
			T_A = -40°C to +85°C			10	
On-Resistance Match Between Channels (Notes 3, 4)	ΔR_{ON}	V_{CC} = 3V, I_{COM} = 10mA, or $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		0.2	0.4	Ω
			T_A = -40°C to +85°C			0.5	
On-Resistance Flatness (Note 5)	R_{FLAT}	V_{CC} = 3V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 1V, 2V, 3V	T_A = +25°C		2.5	3.75	Ω
			T_A = -40°C to +85°C			4	
NO_ or NC_ Off-Leakage Current	I_{OFF}	V_{CC} = 5.5V, $V_{NO\_}$ or $V_{NC\_}$ = 1V or 4.5V, $V_{COM\_}$ = 4.5V or 1V	T_A = +25°C	-2		+2	nA
			T_A = -40°C to +85°C	-10		+10	
COM_ On-Leakage Current	I_{ON}	V_{CC} = 5.5V; $V_{NO\_}$ or $V_{NC\_}$ = 1V, 4.5V, or floating; $V_{COM\_}$ = 1V, 4.5V, or floating	T_A = +25°C	-2		+2	nA
			T_A = -40°C to +85°C	-12.5		+12.5	
DYNAMIC CHARACTERISTICS							
Signal Over Rail to High-Z Switching Time		$V_{NO\_}$ or $V_{NC\_}$ = V_{CC} to (V_{CC} + 0.5V), V_{CC} < 5V (Figure 1)			0.5	1	µs
High-Z to Low-Z Switching Time		$V_{NO\_}$ or $V_{NC\_}$ = (V_{CC} + 0.5V) to V_{CC}, V_{CC} < 5V (Figure 1)			0.5	1	µs
Skew (Note 3)	t_{SKEW}	R_S = 39Ω, C_L = 50pF (Figure 2)			0.15	1	ns
Propagation Delay (Note 3)	t_{PD}	R_S = 39Ω, C_L = 50pF (Figure 2)			0.9	2	ns
Turn-On Time	t_{ON}	V_{CC} = 3V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 300Ω, C_L = 50pF (Figure 1)	T_A = +25°C		40	60	ns
			T_A = -40°C to +85°C			100	
Turn-Off Time	t_{OFF}	V_{CC} = 3V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 300Ω, C_L = 50pF (Figure 1)	T_A = +25°C		30	40	ns
			T_A = -40°C to +85°C			60	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Injection	Q	$V_{COM\_}$ = 1.5V, R_S = 0Ω, C_L = 1nF (Figure 3)		8		pC
Off-Isolation (Note 6)	V_{ISO}	f = 100kHz, $V_{COM\_}$= $1V_{RMS}$, R_L = 50Ω, C_L = 5pF (Figure 4)		-80		dB
Crosstalk	V_{CT}	f = 1MHz, $V_{COM\_}$= $1V_{RMS}$, R_L = 50Ω, C_L = 5pF (Figure 4)		-95		dB
-3dB Bandwidth	BW	Signal = 0dBm, R_L = 50Ω, C_L = 5pF (Figure 4)		150		MHz
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $V_{COM\_}$ = 1V + $2V_{P-P}$, R_L = 600Ω		0.04		%
NO_ Off-Capacitance	C_{OFF}	f = 1MHz (Figure 5)		12		pF
COM On-Capacitance	C_{ON}	f = 1MHz (Figure 5)		27.5		pF
DIGITAL I/O (IN_)						
Input-Logic High Voltage	V_{IH}	V_{CC} = 2V to 3.6V	1.4			V
		V_{CC} = 3.6V to 5.5V	1.8			
Input-Logic Low Voltage	V_{IL}	V_{CC} = 2V to 3.6V			0.5	V
		V_{CC} = 3.6V to 5.5V			0.8	
Input Leakage Current	I_{IN}	$V_{IN\_}$ = 0 or 5.5V	-0.5		+0.5	µA

Note 2: Specifications are 100% tested at T_A = +85°C only, and guaranteed by design and characterization over the specified temperature range.

Note 3: Guaranteed by design and characterization; not production tested.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

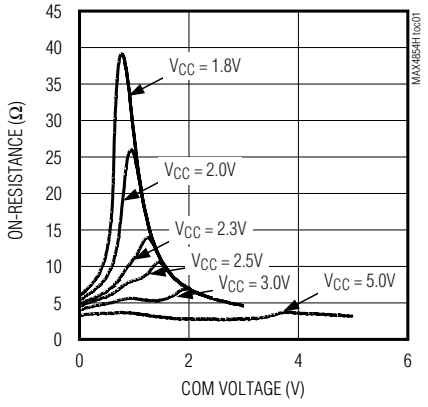
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 6: Off-Isolation = $20\log_{10}$ ($V_{COM\_}$ / $V_{NO\_}$), $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.

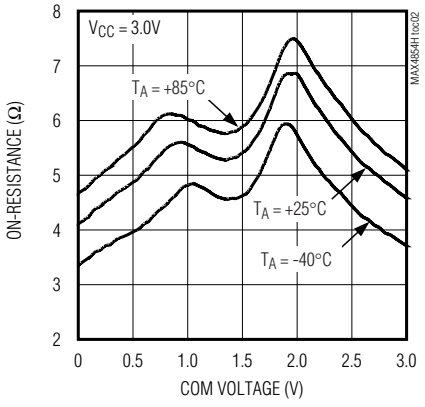
Typical Operating Characteristics

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

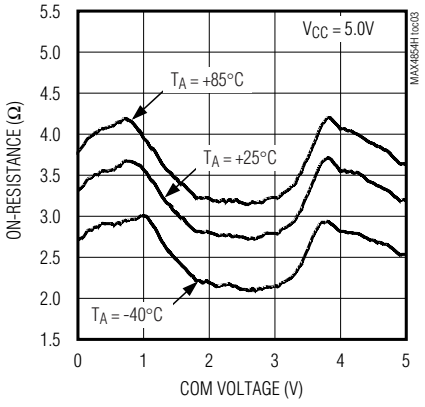
ON-RESISTANCE vs. COM VOLTAGE



ON-RESISTANCE vs. COM VOLTAGE



ON-RESISTANCE vs. COM VOLTAGE

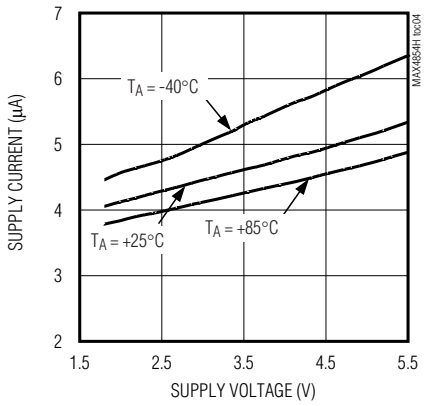


Quad SPST, High-Bandwidth, Signal Line Protection Switch

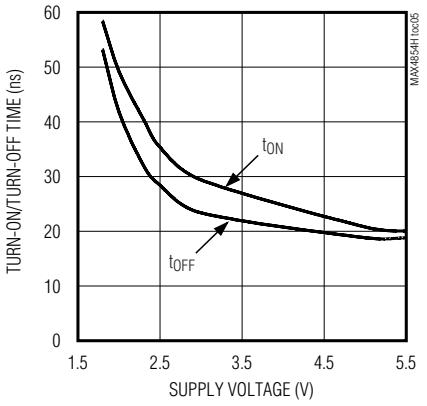
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

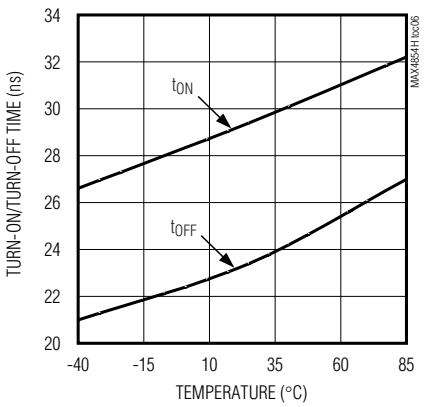
SUPPLY CURRENT vs. SUPPLY VOLTAGE



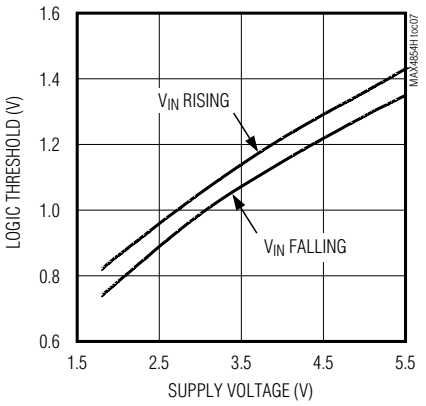
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



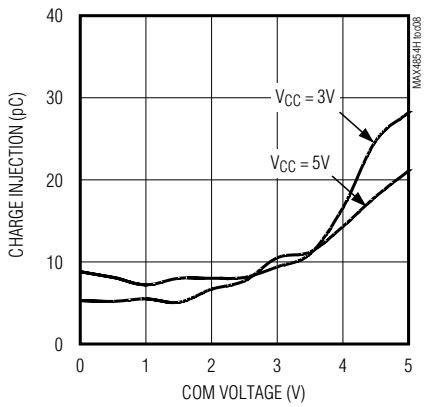
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



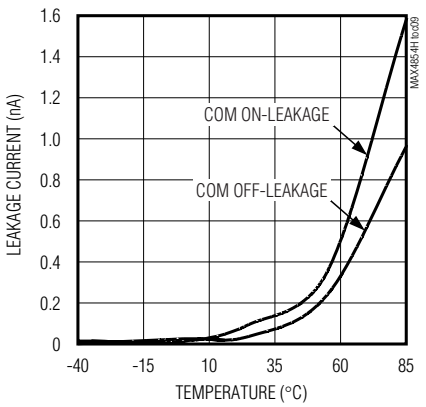
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



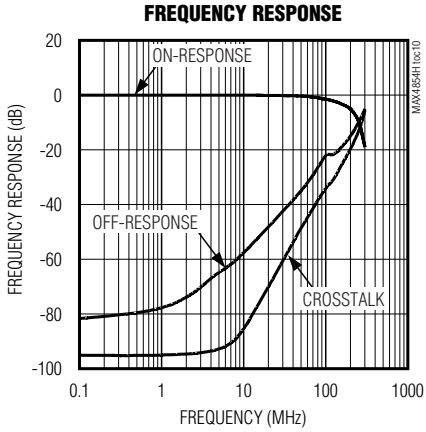
CHARGE INJECTION vs. COM VOLTAGE



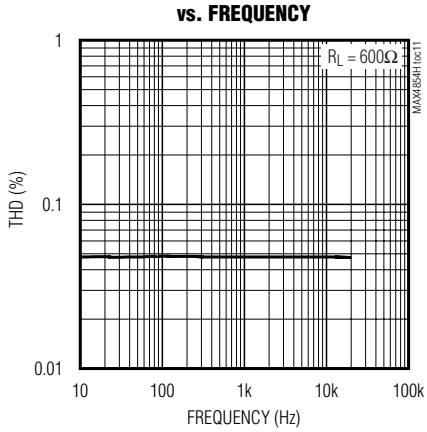
LEAKAGE CURRENT vs. TEMPERATURE



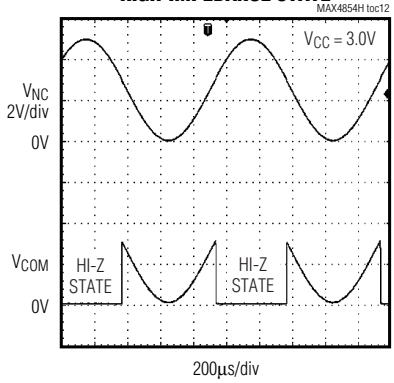
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



SWITCH ENTERING HIGH-IMPEDANCE STATE



Pin Description

PIN	NAME	FUNCTION
1, 5, 7, 10	NO1, NO2, NO3, NO4	Normally Open Terminals for Analog Switch (MAX4854H)
1, 5, 7, 10	NC1, NC2, NC3, NC4	Normally Closed Terminals for Analog Switch (MAX4854HL)
2, 11	N.C.	No Connection. Internally not connected.
3	IN2	Digital Control Input for Analog Switch 2. A logic-low (MAX4854H) or logic-high (MAX4854HL) on IN2 opens switch 2 and a logic-high (MAX4854H) or logic-low (MAX4854HL) on IN2 connects COM2 to NO2.
4	COM2	Common Terminal for Analog Switch 2
6	GND	Ground
8	COM3	Common Terminal for Analog Switch 3
9	IN3	Digital Control Input for Analog Switch 3. A logic-low (MAX4854H) or logic-high (MAX4854HL) on IN3 opens switch 3 and a logic-high (MAX4854H) or logic-low (MAX4854HL) on IN3 connects COM3 to NO3.
12	COM4	Common Terminal for Analog Switch 4
13	IN4	Digital Control Input for Analog Switch 4. A logic-low (MAX4854H) or logic-high (MAX4854HL) on IN4 opens switch 4 and a logic-high (MAX4854H) or logic-low (MAX4854HL) on IN4 connects COM4 to NO4.
14	V_{CC}	Supply Voltage. Bypass V_{CC} to GND with a 0.01µF capacitor as close to the pin as possible.
15	IN1	Digital Control Input for Analog Switch 1. A logic-low (MAX4854H) or logic-high (MAX4854HL) on IN1 opens switch 1 and a logic-high (MAX4854H) or logic-low (MAX4854HL) on IN1 connects COM1 to NO1.
16	COM1	Common Terminal for Analog Switch 1
—	EP	Exposed Paddle. Connect to PC board ground plane.

Detailed Description

The MAX4854H/MAX4854HL quad SPST switches have low on-resistance, operate from a +2V to +5.5V supply, and are fully specified for nominal 3.0V applications. These devices feature overvoltage protection by putting the switch into high-impedance mode when the switch input exceeds V_{CC}.

These switches have low 27.5pF on-channel capacitance, which allows for 12Mbps switching of the data signals for USB 2.0 full speed/1.1 applications. The MAX4854H/MAX4854HL are designed to switch D+ and D- USB signals with a guaranteed skew of less than 1ns (see Figure 2) as measured from 50% of the input signal to 50% of the output signal.

Applications Information

Digital Control Inputs

The logic inputs (IN_) accept up to +5.5V even if the supply voltages are below this level. For example, with a +3.3V V_{CC} supply, IN_ can be driven low to GND and high to +5.5V, allowing for mixing of logic levels in a system. Driving IN_ rail-to-rail minimizes power consumption. For a +2V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 1.8V (high).

Analog Signal Levels

The on-resistance of these switches changes very little for analog input signals across the entire supply voltage range (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_ and COM_ pins can be either inputs or outputs.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current limited.

Quad SPST, High-Bandwidth, Signal Line Protection Switch

Test Circuits/Timing Diagrams

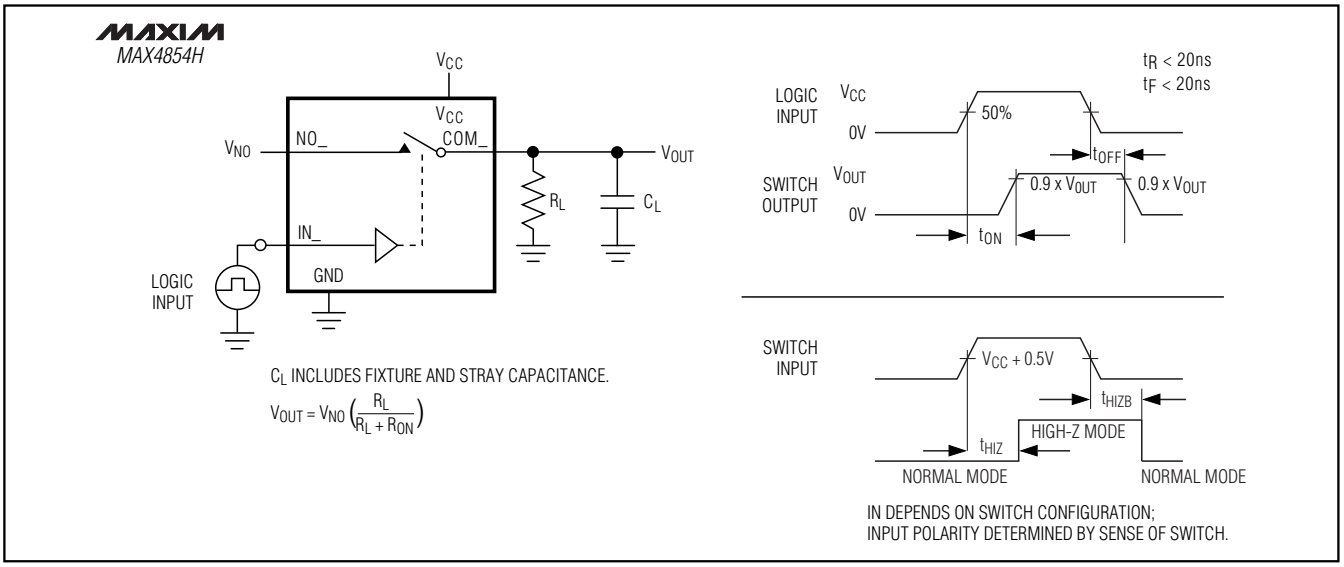


Figure 1. Switching Time

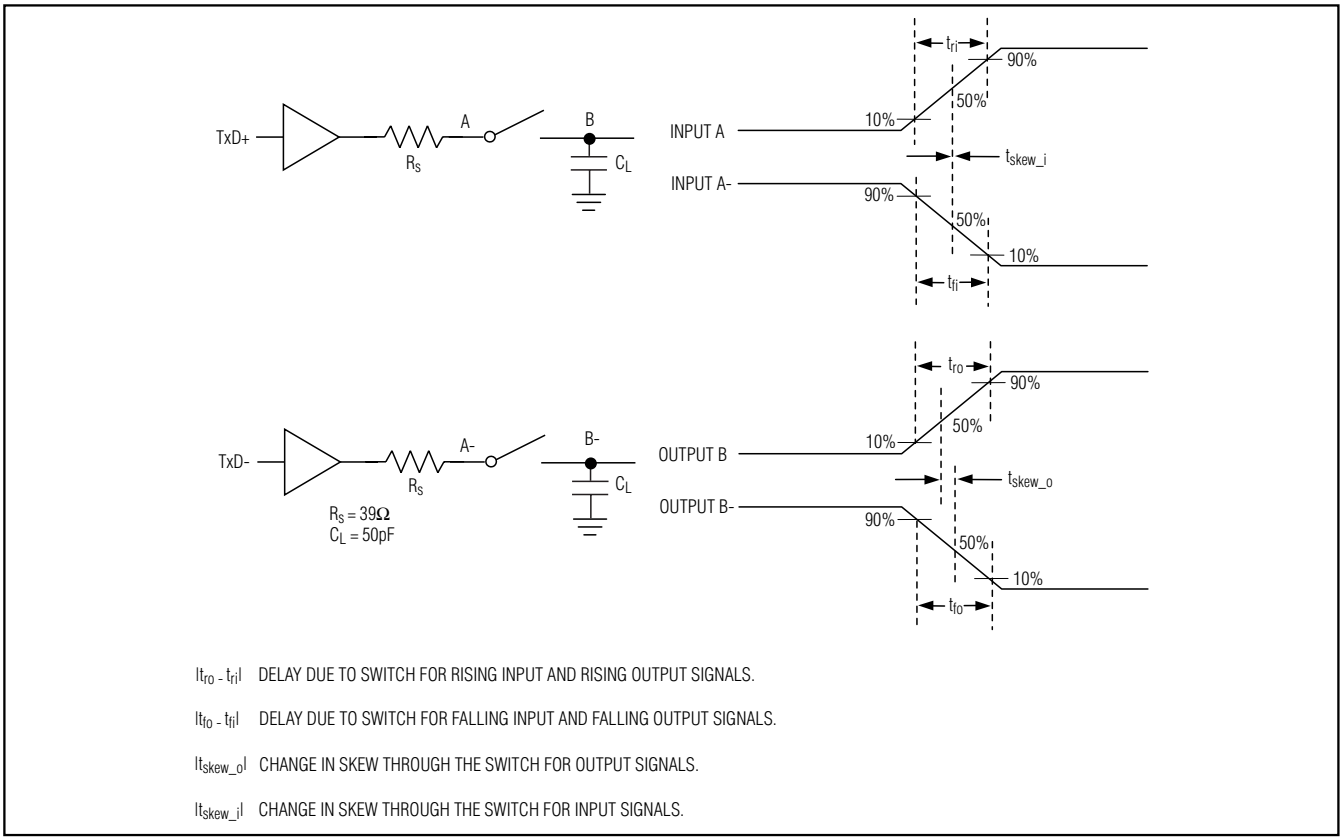


Figure 2. Output Signal Skew

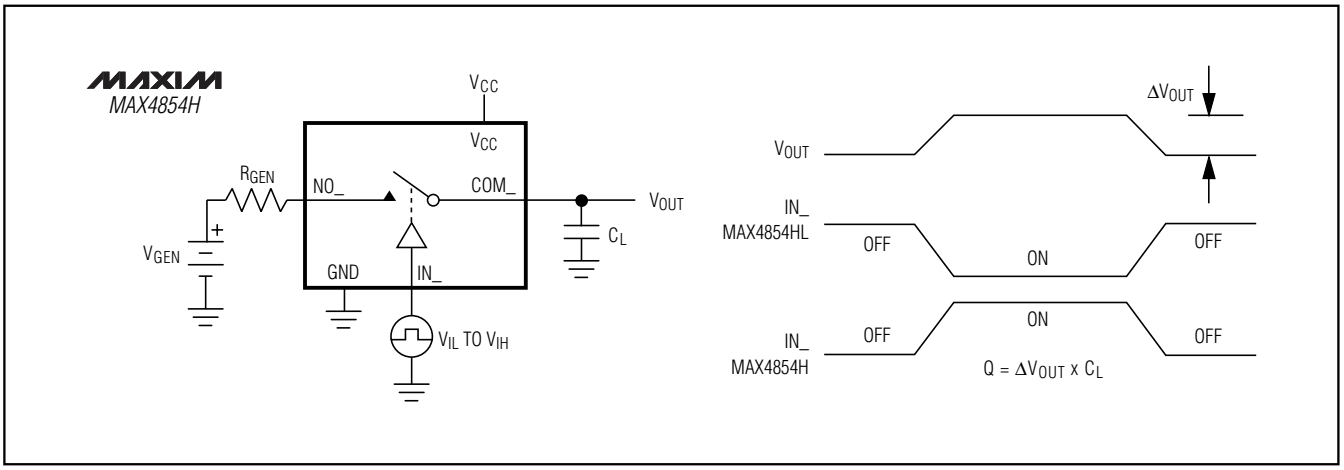


Figure 3. Charge Injection

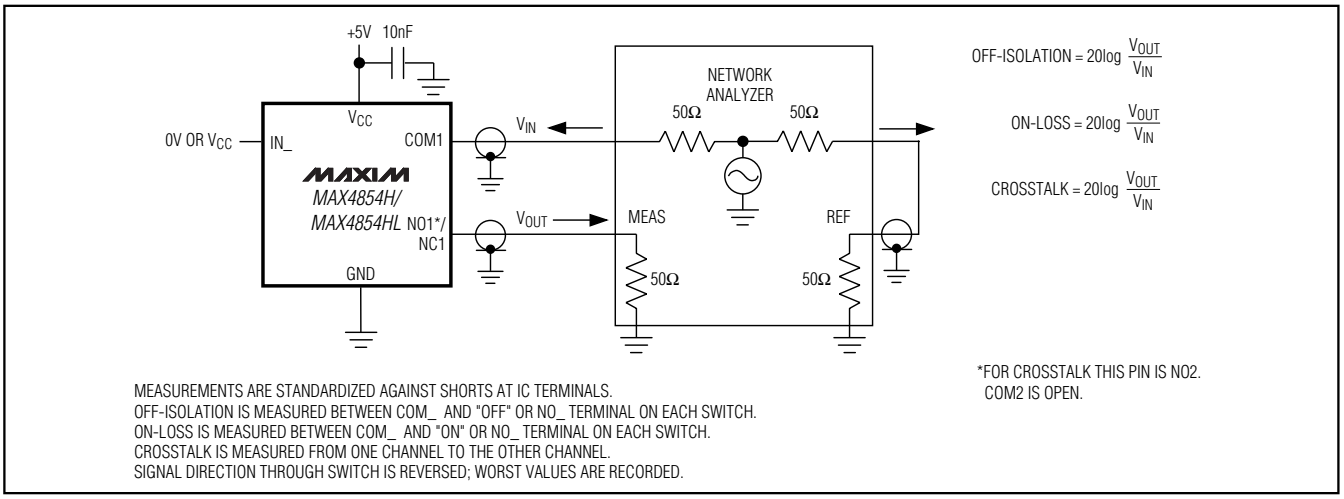


Figure 4. On-Loss, Off-Isolation, and Crosstalk

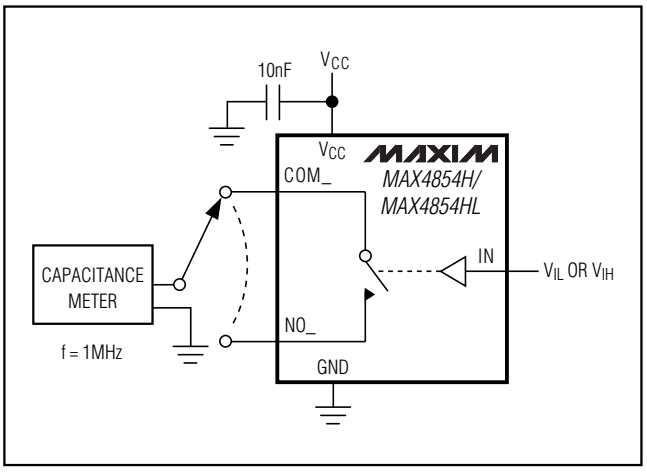


Figure 5. Channel Off-/On-Capacitance

Chip Information

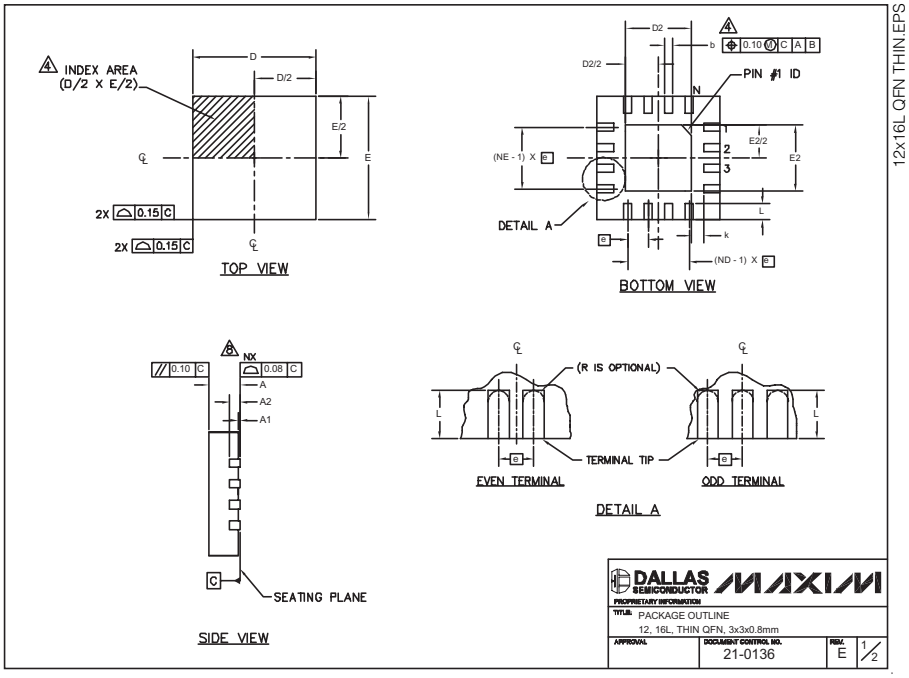
TRANSISTOR COUNT: 735

PROCESS: CMOS

Quad SPST, High-Bandwidth, Signal Line Protection Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.85	0.90	0.95	0.85	0.90	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12, 16L, THIN QFN, 3x3x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0136
REV. E
2/2