ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74HC165
Integrated Circuit
TTL – High Speed CMOS,
8–Bit Parallel–In/Serial–Out Shift Register

Description:

The NTE74HC165 is an 8–bit parallel–in/serial–out shift register in a 16–Lead DIP type package that utilize advanced silicon–gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits along with the ability to drive 10 LS–TTL loads.

This 8–bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2–input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of th CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is HIGH. When taken LOW, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

The 74HC logic family is functionally as well as pin–out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and GND.

Features:

- Typical Propagation Delay: Clock to Q: 20ns
- Low Quiescent Current: 80μA (max)
- Low Input Current: 1μA (max)
- Wide Power Supply Range: 2V to 6V
- Fanout to 10 LS–TTL Loads

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–55	–	+85	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics: (Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C	T_A = –40° to +85°C		Unit
					Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum Low Level Input Voltage	V_{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\| \le 20\mu A$	–	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			$\|I_{OUT}\| \le 4.0mA$	4.5	4.2	3.98	3.84	V
			$\|I_{OUT}\| \le 5.2mA$	6.0	5.7	5.48	5.34	V
Minimum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	$\|I_{OUT}\| \le 20\mu A$	–	0	0.1	0.1	V
			$\|I_{OUT}\| \le 4.0mA$	4.5	0.2	0.26	0.33	V
			$\|I_{OUT}\| \le 5.2mA$	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	–	8.0	80	μA

Note 4. For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively (The V_{IH} value at 5.5V is 3.85V). The worst case leakage current (I_{IN}, I_{CC} and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics: (V_{CC} = 5V, t_r = t_f = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Operating Frequency	f_{MAX}		50	30	ns
Maximum Propagation Delay (H to Q_H or $\overline{Q}_H$)	t_{PHL}, t_{PLH}		15	25	ns
Maximum Propagation Delay (Serial Shift/Parallel Load to Q_H)	t_{PHL}, t_{PLH}		13	25	ns
Maximum Propagation Delay (Clock to Output)	t_{PHL}, t_{PLH}		15	25	ns
Minimum Set Up Time (Serial Input to Clock, Parallel or Data to Shift/Load)	t_S		10	20	ns

AC Electrical Characteristics (Cont'd): (V_{CC} = 5V, $t_r = t_f$ = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Minimum Set Up Time (Shift/Load to Clock)	t_S		11	20	ns
Minimum Set Up Time (Clock Inhibit to Clock)	t_S		10	20	ns
Minimum Hold Time (Serial Input to Clock or Parallel Data to Shift/Load)	t_H		–	0	ns
Minimum Pulse Width (Clock)	t_W		–	16	ns

AC Electrical Characteristics: ($t_r = t_f$ = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Maximum Operating Frequency	f_{MAX}		2.0	–	5	4	MHz
			4.5	–	27	21	MHz
			6.0	–	32	25	MHz
Maximum Propagation Delay (Delay H to Q_H or $\overline{Q}_H$)	t_{PHL}, t_{PLH}		2.0	70	150	189	ns
			4.5	21	30	38	ns
			6.0	18	26	33	ns
Maximum Propagation Delay (Delay Serial Shift/Parallel Load to Q_H)	t_{PHL}, t_{PLH}		2.0	70	175	220	ns
			4.5	21	35	44	ns
			6.0	18	30	37	ns
Maximum Propagation Delay (Delay Clock to Output)	t_{PHL}, t_{PLH}		2.0	70	150	189	ns
			4.5	21	30	38	ns
			6.0	18	26	33	ns
Minimum Setup Time (Serial Input to Clock, or Parallel Data to Shift/Load)	t_S		2.0	35	100	125	ns
			4.5	11	20	25	ns
			6.0	9	17	21	ns
Minimum Setup Time (Shift/Load to Clock)	t_S		2.0	38	100	125	ns
			4.5	12	20	25	ns
			6.0	9	17	21	ns
Minimum Setup Time (Clock Inhibit to Clock)	t_S		2.0	35	100	125	ns
			4.5	11	20	25	ns
			6.0	9	17	21	ns
Minimum Hold Time (Serial Input to Clock, or Parallel Data to Shift/Load)	t_H		2.0	0	0	0	ns
			4.5	0	0	0	ns
			6.0	0	0	0	ns
Minimum Pulse Width, Clock	t_W		2.0	30	80	100	ns
			4.5	9	16	20	ns
			6.0	8	14	18	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		2.0	30	75	95	ns
			4.5	9	15	19	ns
			6.0	8	13	16	ns

AC Electrical Characteristics (Cont'd): ($t_r = t_f = 6ns$, $C_L = 50pF$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25°C$	$T_A = -40°$ to $+85°C$		Unit
				Typ	Guaranteed Limits		
Maximum Input Rise and Fall Time	t_r, t_f		2.0	–	1000	1000	ns
			4.5	–	500	500	ns
			6.0	–	400	400	ns
Power Dissipation Capacitance	C_{PD}	Per Package, Note 5	–	100	–	–	pF
Maximum Input Capacitance	C_{IN}		–	5	10	10	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_A	Q_H
L	X	X	X	a . . .h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = HIGH Level (Steady State)

L = LOW Level (Steady State)

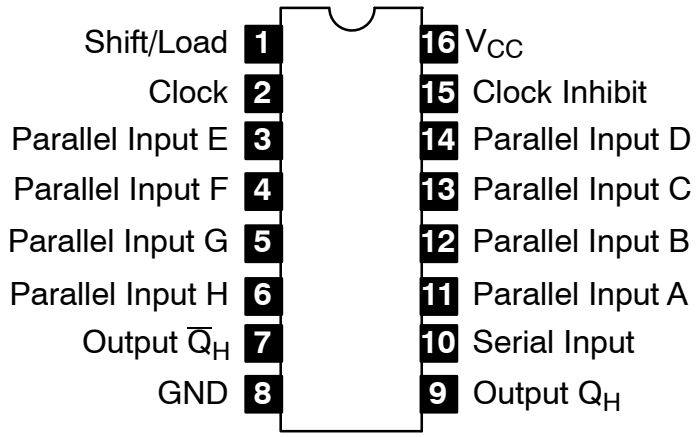
X = Irrelevant (any input, including transitions)

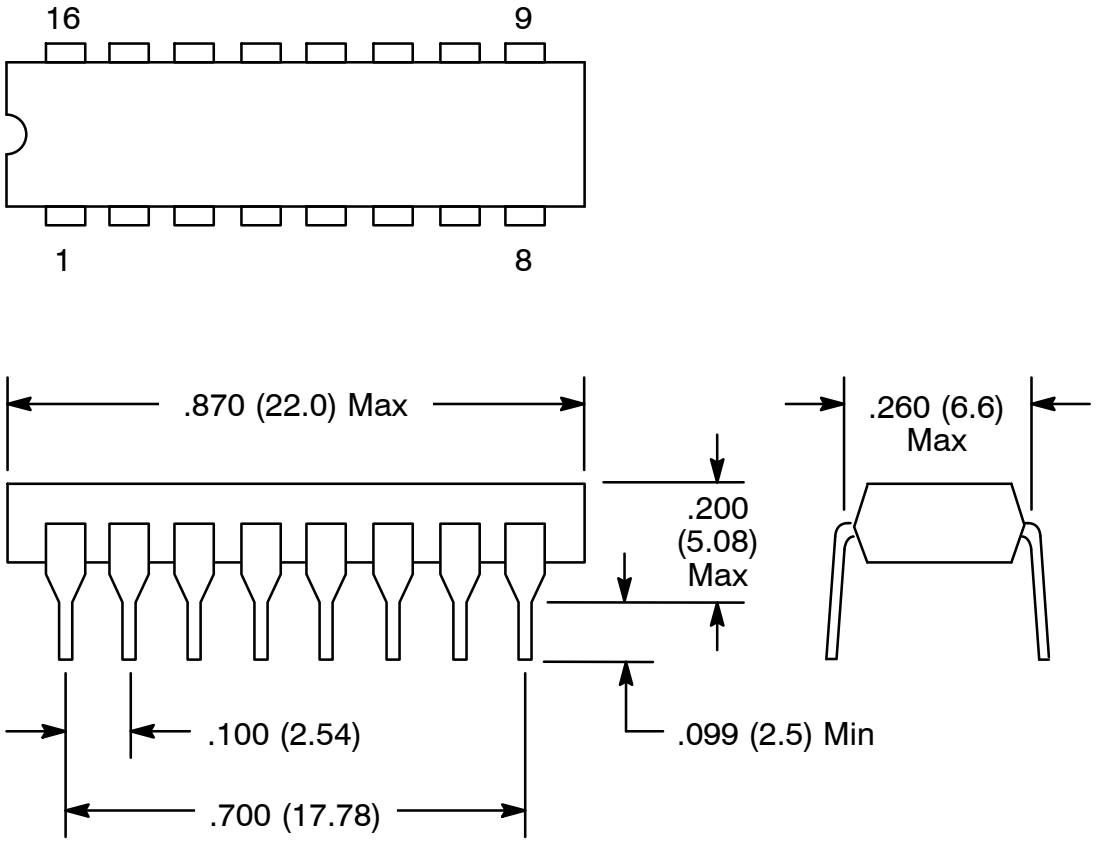
↑ = Transition from LOW−to−HIGH level

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{AN}, Q_{GN} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one−bit shift.

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)