



FSB50325S

Smart Power Module (SPM®)

Features

- 250V 1.5A 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- Surface mounted device package
- Moisture Sensitive Level (MSL) 3

General Description

FSB50325S is a tiny smart power module (SPM®) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB50325S provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB50325S is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.

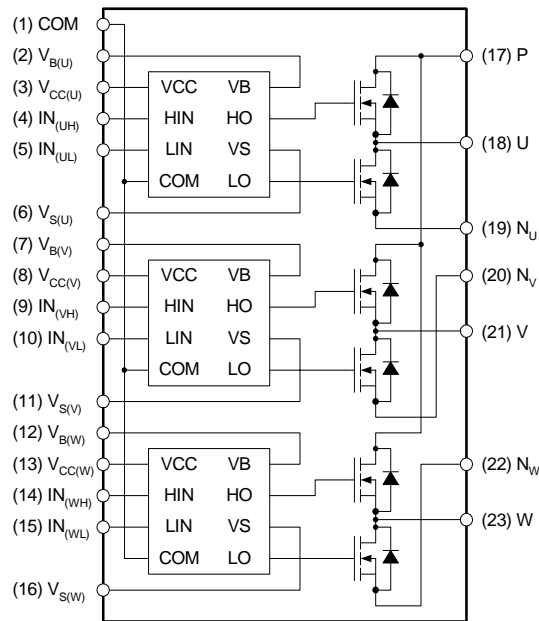


Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		250	V
I_{D25}	Each FRFET Drain Current, Continuous	$T_C = 25^\circ\text{C}$	1.5	A
I_{D80}	Each FRFET Drain Current, Continuous	$T_C = 80^\circ\text{C}$	1.0	A
I_{DP}	Each FRFET Drain Current, Peak	$T_C = 25^\circ\text{C}$, $PW < 100\mu\text{s}$	3.0	A
P_D	Maximum Power Dissipation	$T_C = 25^\circ\text{C}$, Each FRFET	10	W
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}-U$, $V_{B(V)}-V$, $V_{B(W)}-W$	20	V
V_{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ $V_{CC}+0.3$	V
T_J	Operating Junction Temperature		-20 ~ 150	$^\circ\text{C}$
T_{STG}	Storage Temperature		-50 ~ 150	$^\circ\text{C}$
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	10.2	$^\circ\text{C/W}$
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V_{rms}

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	$V_{S(U)}$	Bias Voltage Ground for U Phase High Side FRFET Driving
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	$V_{S(V)}$	Bias Voltage Ground for V Phase High Side FRFET Driving
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	$V_{S(W)}$	Bias Voltage Ground for W Phase High Side FRFET Driving
17	P	Positive DC-Link Input
18	U	Output for U Phase
19	N_U	Negative DC-Link Input for U Phase
20	N_V	Negative DC-Link Input for V Phase
21	V	Output for V Phase
22	N_W	Negative DC-Link Input for W Phase
23	W	Output for W Phase



Note:

Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside SPM®. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Electrical Characteristics (T_J = 25°C, V_{CC}=V_{BS}=15V Unless Otherwise Specified)

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{IN} = 0V, I _D = 250μA (Note 2)	250	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.31	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0V, V _{DS} = 250V	-	-	250	μA
R _{DS(on)}	Static Drain-Source On-Resistance	V _{CC} = V _{BS} = 15V, V _{IN} = 5V, I _D = 1.0A	-	1.4	1.8	Ω
V _{SD}	Drain-Source Diode Forward Voltage	V _{CC} = V _{BS} = 15V, V _{IN} = 0V, I _D = -1.0A	-	-	1.2	V
t _{ON}	Switching Times	V _{PN} = 150V, V _{CC} = V _{BS} = 15V, I _D = 1.0A V _{IN} = 0V ↔ 5V Inductive load L=3mH High- and low-side FRFET switching (Note 3)	-	1076	-	ns
t _{OFF}			-	660	-	ns
t _{rr}			-	108	-	ns
E _{ON}			-	47	-	μJ
E _{OFF}			-	3.1	-	μJ
RBSOA	Reverse-bias Safe Operating Area	V _{PN} = 200V, V _{CC} = V _{BS} = 15V, I _D = I _{DP} , V _{DS} =BV _{DSS} , T _J = 150°C High- and low-side FRFET switching (Note 4)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{QCC}	Quiescent V _{CC} Current	V _{CC} =15V, V _{IN} =0V Applied between V _{CC} and COM	-	-	160	μA
I _{QBS}	Quiescent V _{BS} Current	V _{BS} =15V, V _{IN} =0V Applied between V _{B(U)} -U, V _{B(V)} -V, V _{B(W)} -W	-	-	100	μA
UV _{CCD}	Low-side Undervoltage Protection (Figure 6)	V _{CC} Undervoltage Protection Detection Level	7.4	8.0	9.4	V
UV _{CCR}		V _{CC} Undervoltage Protection Reset Level	8.0	8.9	9.8	V
UV _{BSD}	High-side Undervoltage Protection (Figure 7)	V _{BS} Undervoltage Protection Detection Level	7.4	8.0	9.4	V
UV _{BSR}		V _{BS} Undervoltage Protection Reset Level	8.0	8.9	9.8	V
V _{IH}	ON Threshold Voltage	Logic High Level	3.0	-	-	V
V _{IL}	OFF Threshold Voltage	Logic Low Level				
I _{IH}	Input Bias Current	V _{IN} = 5V	-	10	20	μA
I _{IL}		V _{IN} = 0V	-	-	2	μA

Note:

- For the measurement point of case temperature T_C, please refer to Figure 3 in page 4.
- BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM®. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.
- t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.
- The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSB50325S	FSB50325S	SPM23BA	330mm	Tape & reel	450

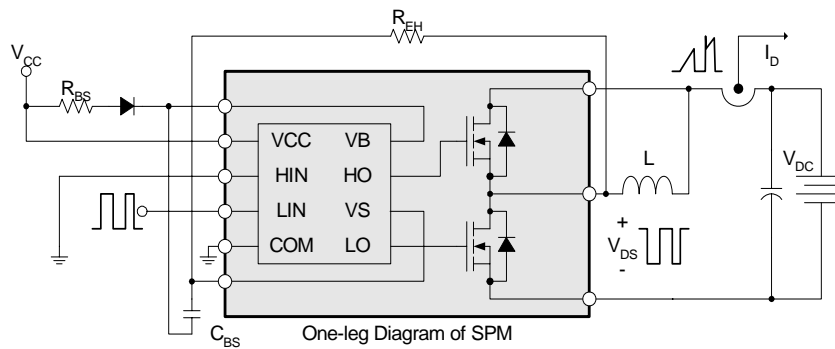
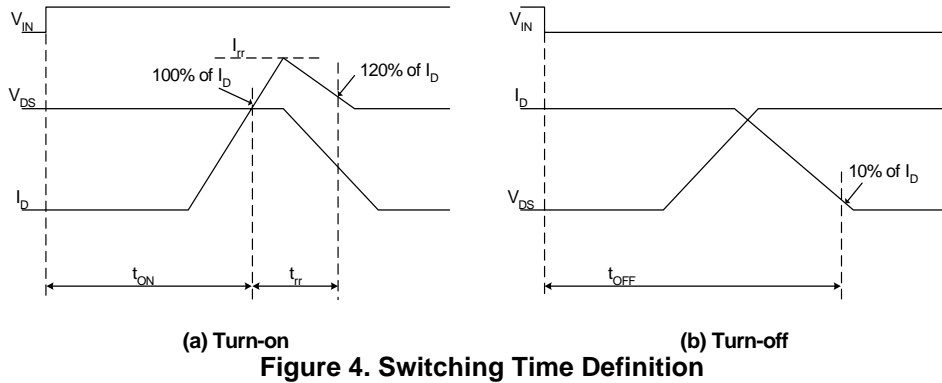


Figure 5. Switching and RBSOA(Single-pulse) Test Circuit (Low-side)

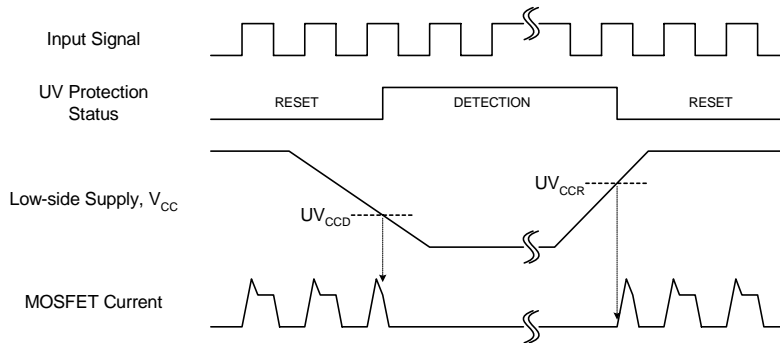


Figure 6. Undervoltage Protection (Low-side)

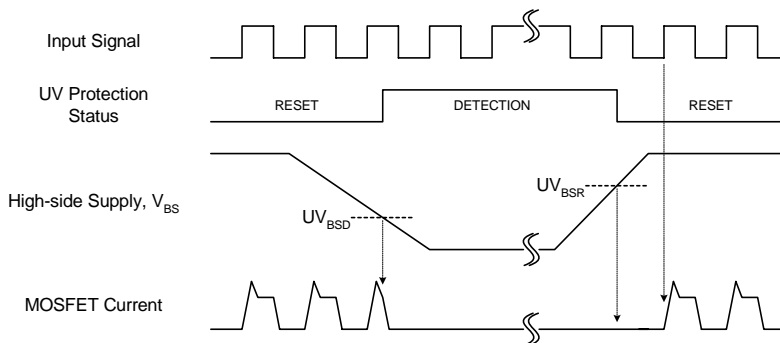


Figure 7. Undervoltage Protection (High-side)

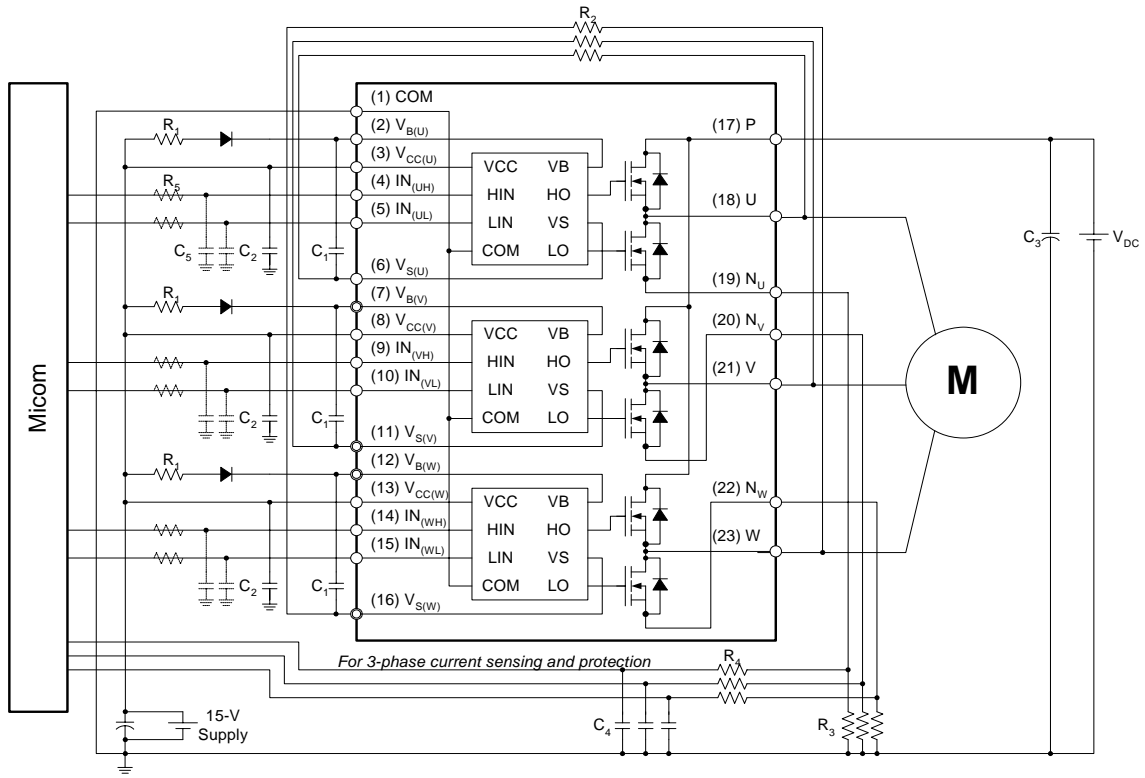
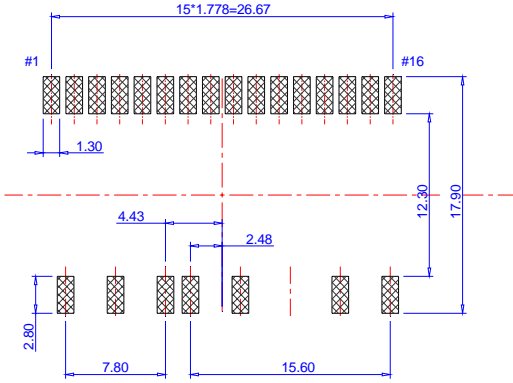
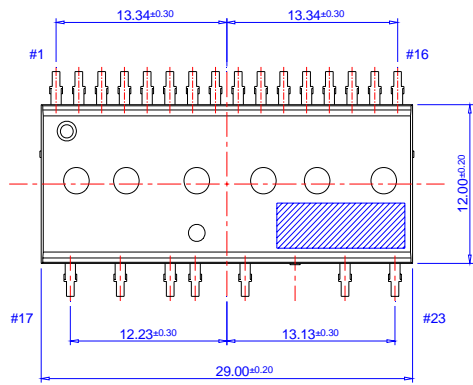
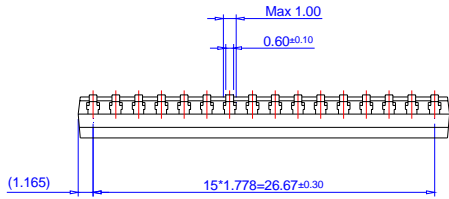
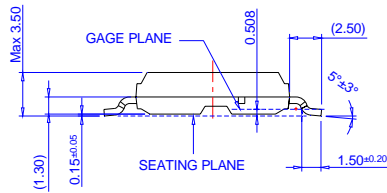
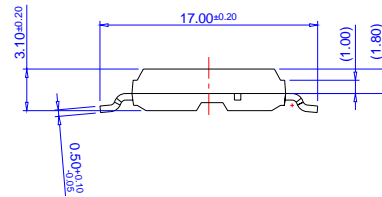
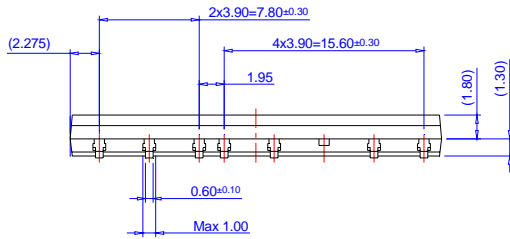


Figure 8. Example of Application Circuit

Detailed Package Outline Drawings



LAND PATTERN RECOMMENDATIONS





TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx®	HiSeC™	Power-SPM™	TinyBuck™
Across the board. Around the world.™	<i>i-Lo</i> ™	PowerTrench®	TinyLogic®
ActiveArray™	ImpliedDisconnect™	Programmable Active Droop™	TINYOPTO™
Bottomless™	IntelliMAX™	QFET®	TinyPower™
Build it Now™	ISOPLANAR™	QS™	TinyWire™
CoolFET™	MICROCOUPLER™	QT Optoelectronics™	TruTranslation™
CorePLUS™	MicroPak™	Quiet Series™	µSerDes™
CROSSVOLT™	MICROWIRE™	RapidConfigure™	UHC®
CTL™	Motion-SPM™	RapidConnect™	UniFET™
Current Transfer Logic™	MSX™	ScalarPump™	VCX™
DOME™	MSXPro™	SMART START™	Wire™
E ² C MOS™	OCX™	SPM®	
EcoSPARK®	OCXPro™	STEALTH™	
EnSigna™	OPTOLOGIC®	SuperFET™	
FACT Quiet Series™	OPTOPLANAR®	SuperSOT™-3	
FACT®	PACMAN™	SuperSOT™-6	
FAST®	PDP-SPM™	SuperSOT™-8	
FASTr™	POP™	SyncFET™	
FPS™	Power220®	TCM™	
FRFET®	Power247®	The Power Franchise®	
GlobalOptoisolator™	PowerEdge™	U™	
GTO™	PowerSaver™	TinyBoost™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I27