

## Power MOSFET



N-Channel MOSFET

### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

Marking code: FA

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.20
$Q_g$ max. (nC)	11
$Q_{gs}$ (nC)	3.1
$Q_{gd}$ (nC)	5.8
Configuration	Single

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHFL014TR-GE3 <sup>a</sup> IRFL014TRPbF-BE3 <sup>a, b</sup>
Lead (Pb)-free	IRFL014TRPbF <sup>a</sup>

#### Notes

- See device orientation
- “-BE3” denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	60	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current <sup>a</sup>	$I_{DM}$	22	W/ $^\circ\text{C}$
Linear derating factor		0.025	
Linear derating factor (PCB mount) <sup>e</sup>		0.017	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	100	mJ
Maximum power dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	W
		$T_A = 25\text{ }^\circ\text{C}$	
Maximum power dissipation (PCB mount) <sup>e</sup>		2.0	
Peak diode recovery dv/dt <sup>c</sup>	dV/dt	4.5	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 16\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.7\text{ A}$  (see fig. 12)
- $I_{SD} \leq 10\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	60	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	-	40	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		60	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.068	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.6 A <sup>b</sup>	-	-	0.20	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 1.6 A		1.9	-	-	S
<b>Dynamic</b>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	300	-	pF
Output capacitance	C <sub>oss</sub>			-	160	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	29	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, V <sub>DS</sub> = 48 V, see fig. 6 and 13 <sup>b</sup>	-	-	11	nC
Gate-source charge	Q <sub>gs</sub>			-	-	3.1	
Gate-drain charge	Q <sub>gd</sub>			-	-	5.8	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10 A, R <sub>g</sub> = 24 Ω, R <sub>D</sub> = 2.7 Ω, see fig. 10 <sup>b</sup>		-	10	-	ns
Rise time	t <sub>r</sub>			-	50	-	
Turn-off delay time	t <sub>d(off)</sub>			-	13	-	
Fall time	t <sub>f</sub>			-	19	-	
Internal drain inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal source inductance	L <sub>S</sub>			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.7	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	22	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 2.7 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.6	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 10 A, dI/dt = 100 A/μs <sup>b</sup>		-	70	140	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	0.20	0.40	
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

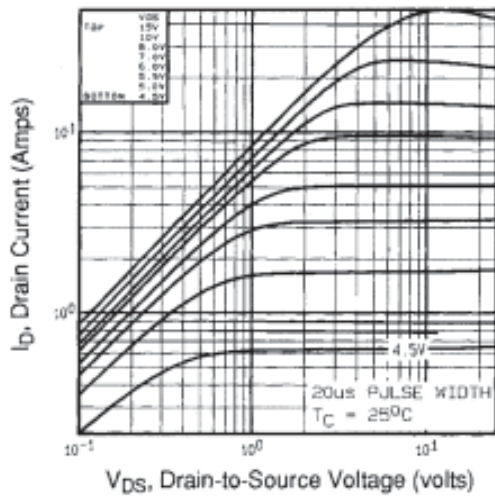


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

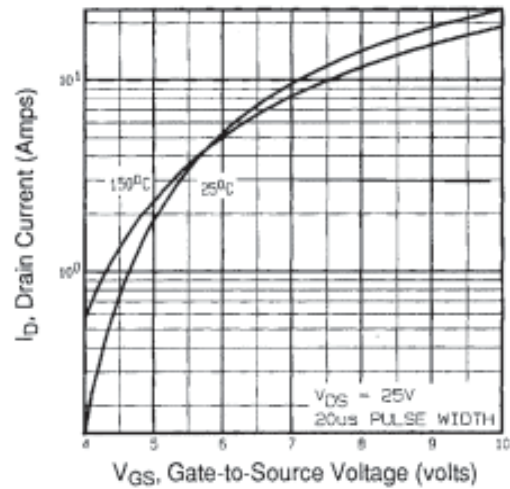


Fig. 3 - Typical Transfer Characteristics



Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$



Fig. 4 - Normalized On-Resistance vs. Temperature

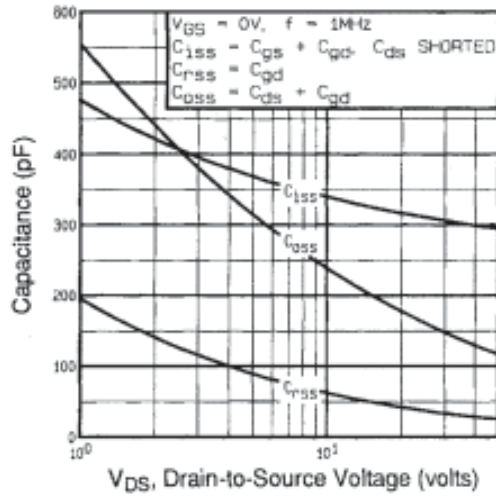


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

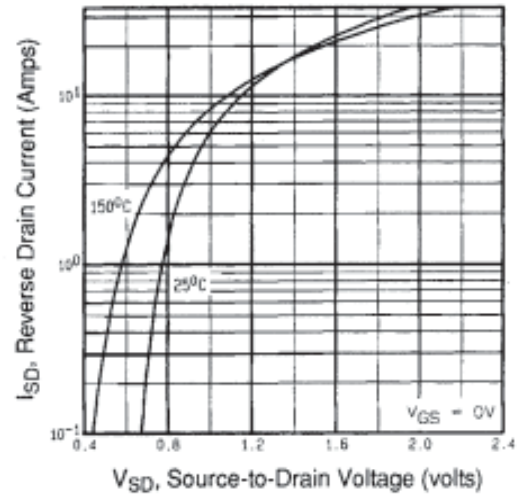


Fig. 7 - Typical Source-Drain Diode Forward Voltage

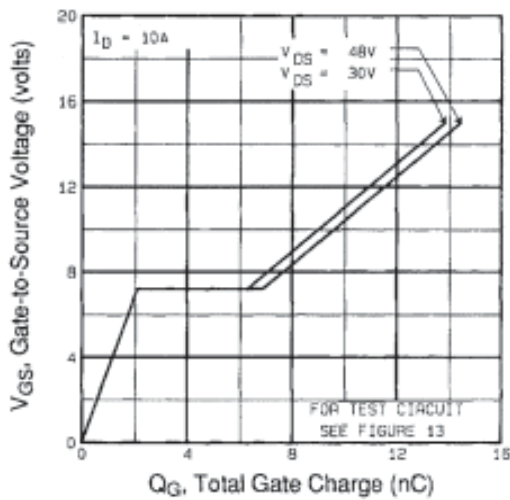


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

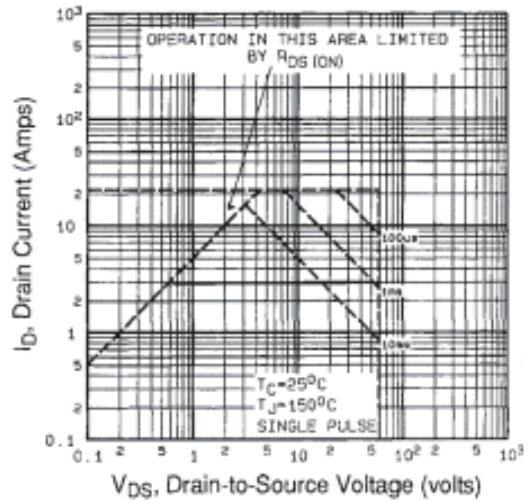


Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a -Switching Time Test Circuit

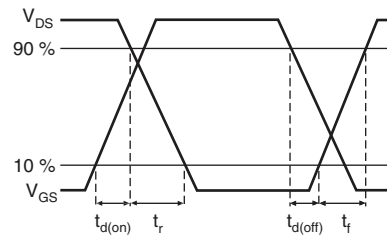


Fig. 10b -Switching Time Waveforms

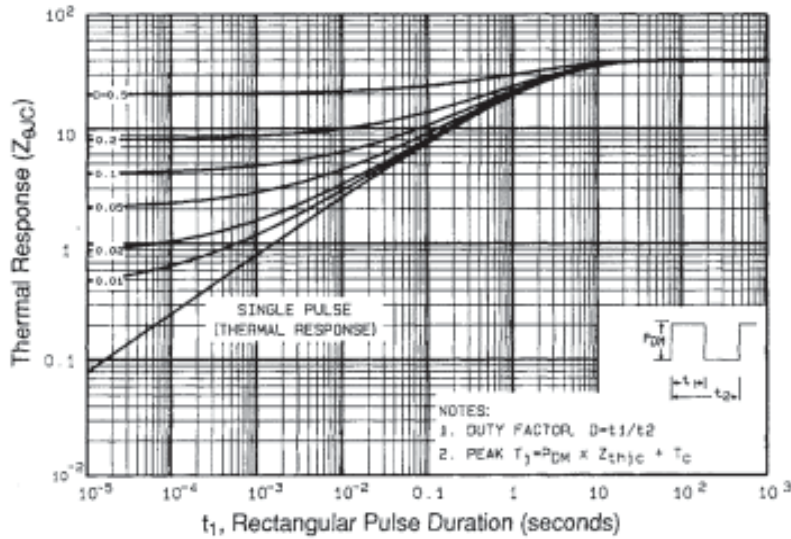


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

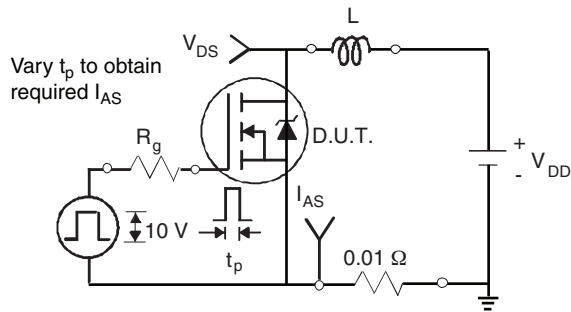


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

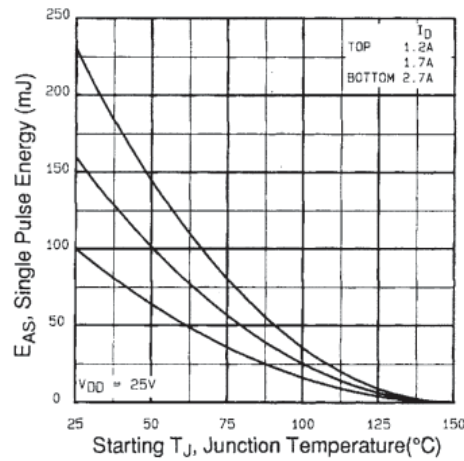


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

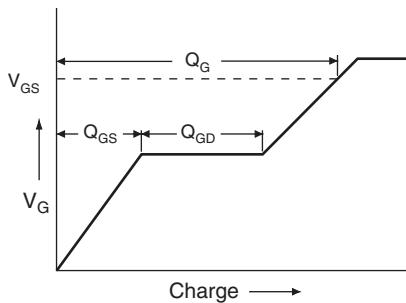


Fig. 13a - Basic Gate Charge Waveform

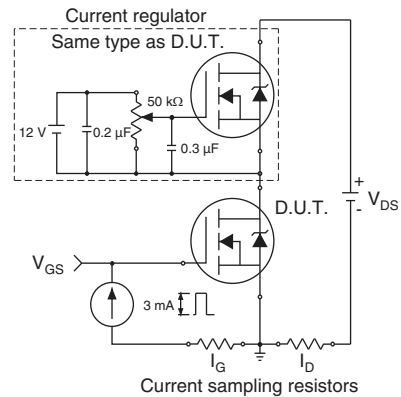


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

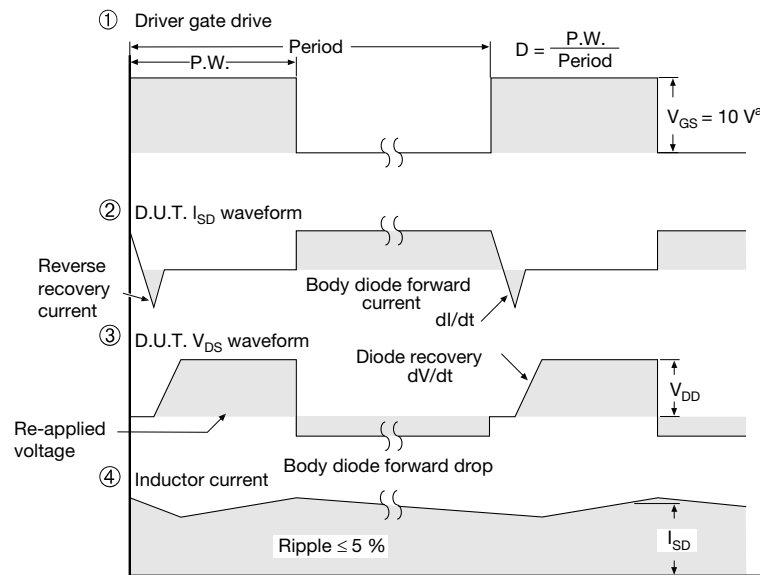
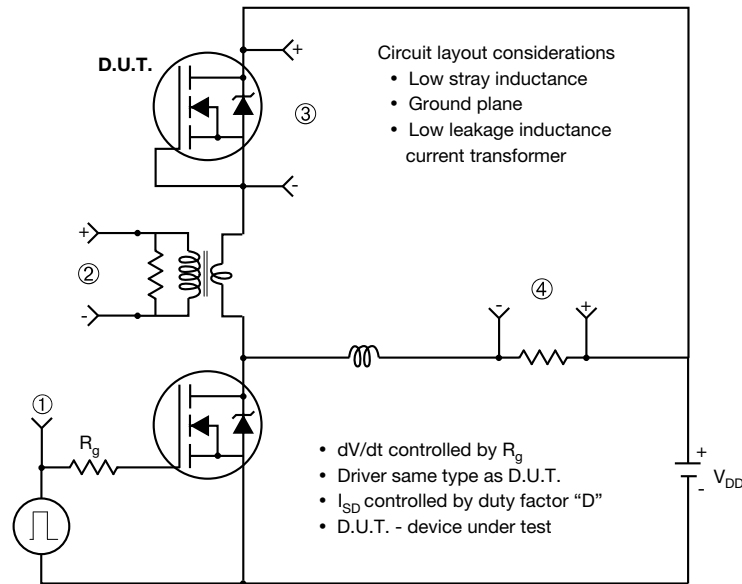
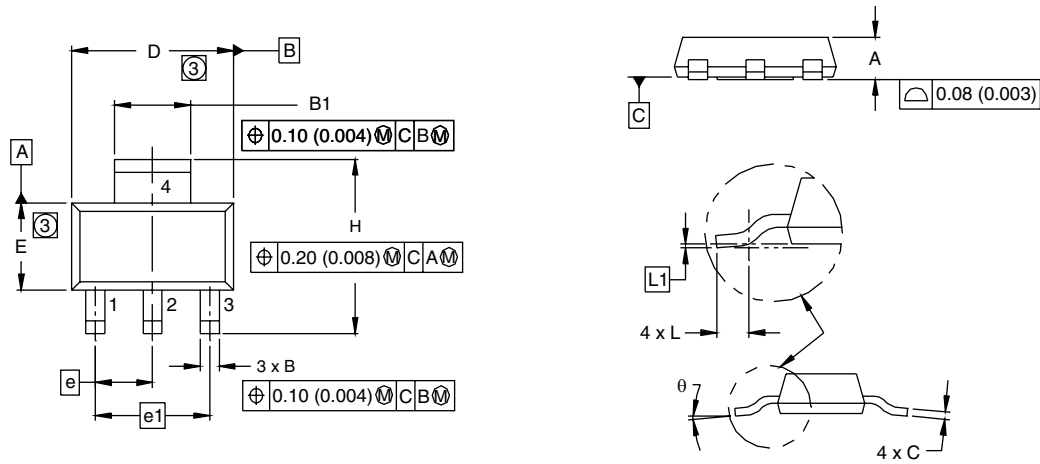


Fig. 12 - For N-Channel

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## SOT-223 (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
$\theta$	-	10°	-	10°
ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969				

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.





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