

**3A, 500V**

## Integrated Power Module for Small Appliance Motor Drive Applications

### Description

IRSM836-035MB is a 3A, 500V Integrated Power Module (IPM) designed for advanced appliance motor drive applications such as energy efficient fans and pumps. IR's technology offers an extremely compact, high performance AC motor-driver in an isolated package. This advanced IPM offers a combination of IR's low  $R_{DS(on)}$  Trench MOSFET technology and the industry benchmark 3-phase high voltage, rugged driver in a small PQFN package. At only 12x12mm and featuring integrated bootstrap functionality, the compact footprint of this surface-mount package makes it suitable for applications that are space-constrained. Integrated over-current protection, fault reporting and under-voltage lockout functions deliver a high level of protection and fail-safe operation. IRSM836-035MB functions without a heat sink.

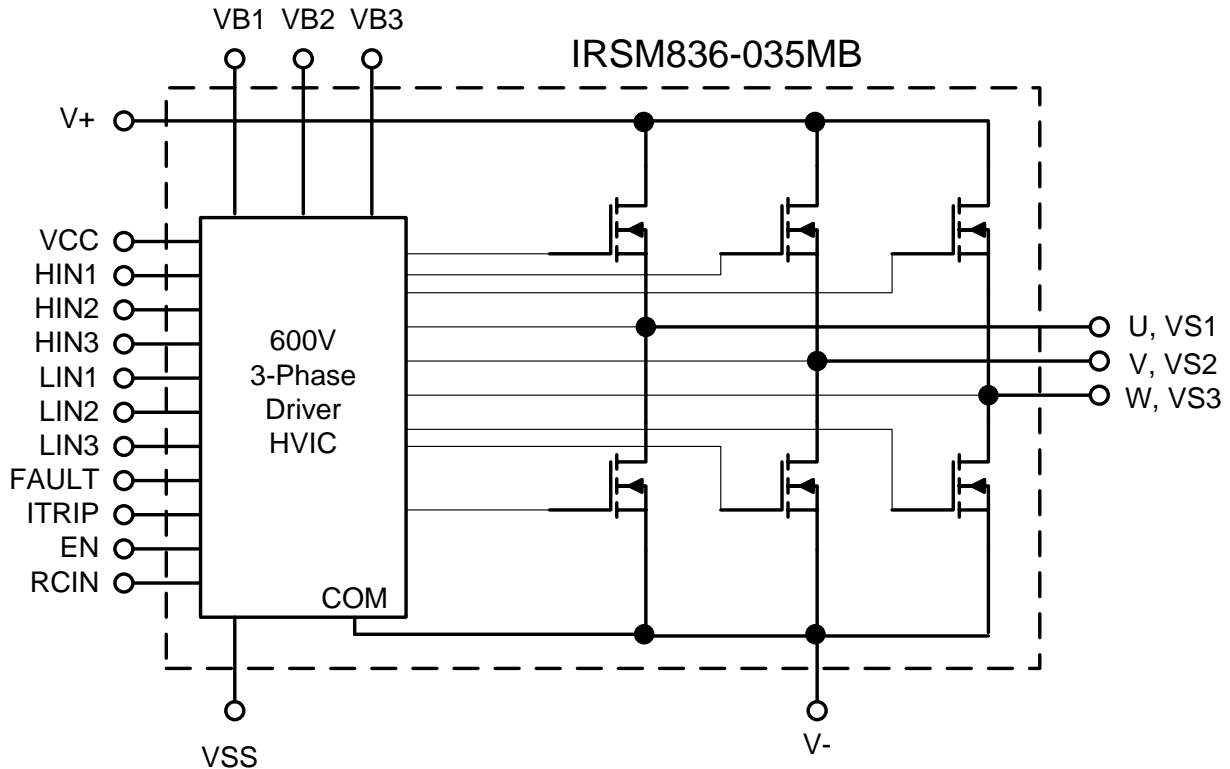
### Features

- Integrated gate drivers and bootstrap functionality
- Suitable for single shunt sensing
- Protection shutdown pin
- Low  $R_{DS(on)}$  Trench FREDFET
- Under-voltage lockout for all channels
- Matched propagation delay for all channels
- Optimized dV/dt for loss and EMI trade offs
- 3.3V Schmitt-triggered active high input logic
- Cross-conduction prevention logic
- Motor power range up to ~110W, without heat sink
- Isolation 1500VRMS min



Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRSM836-035MB	27L PQFN 12 x 12 mm	Tape and Reel	2000	IRSM836-035MBTR
		Tray	800	IRSM836-035MB

All part numbers are PbF

**Internal Electrical Schematic**

**Absolute Maximum Ratings**

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to VSS unless otherwise stated in the table.

Symbol	Description	Min	Max	Unit
$BV_{DSS}$	MOSFET Blocking Voltage	---	500	V
$I_o @ T=25^{\circ}C$	DC Output Current per MOSFET	---	3	A
$I_{OP}$	Pulsed Output Current (Note 1)	---	20	
$P_d @ T_C=25^{\circ}C$	Maximum Power Dissipation per MOSFET	---	36	W
$V_{ISO}$	Isolation Voltage (1min) (Note 2)	---	1500	$V_{RMS}$
$T_J$	Operating Junction Temperature	-40	150	$^{\circ}C$
$T_L$	Lead Temperature (Soldering, 30 seconds)	---	260	$^{\circ}C$
$T_S$	Storage Temperature	-40	150	$^{\circ}C$
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	$V_{B1,2,3} - 20$	$V_{B1,2,3} + 0.3$	V
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	500	V
$V_{CC}$	Low Side and Logic Supply voltage	-0.3	20	V
$V_{IN}$	Input Voltage of LIN, HIN, $I_{TRIP}$ , EN, RCIN, FLT	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V

Note 1: Pulse Width = 100 $\mu$ s,  $T_C = 25^{\circ}C$ , Duty=1%.

Note 2: Characterized, not tested at manufacturing

## Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V+	Positive DC Bus Input Voltage	---	400	V
V <sub>S1,2,3</sub>	High Side Floating Supply Offset Voltage	(Note 3)	400	V
V <sub>B1,2,3</sub>	High Side Floating Supply Voltage	V <sub>S</sub> +12	V <sub>S</sub> +20	V
V <sub>CC</sub>	Low Side and Logic Supply Voltage	13.5	16.5	V
V <sub>IN</sub>	Input Voltage of LIN, HIN, I <sub>TRIP</sub> , EN, FLT	0	5	V
F <sub>p</sub>	PWM Carrier Frequency	---	20	kHz

The Input/Output logic diagram is shown in Figure 1. For proper operation the module should be used within the recommended conditions. All voltages are absolute referenced to COM. The V<sub>S</sub> offset is tested with all supplies biased at 15V differential.

Note 3: Logic operational for V<sub>S</sub> from COM-5V to COM+250V. Logic state held for V<sub>S</sub> from COM-5V to COM-V<sub>BS</sub>.

## Static Electrical Characteristics

(V<sub>CC</sub>-COM) = (V<sub>B</sub>-V<sub>S</sub>) = 15 V. T<sub>A</sub> = 25°C unless otherwise specified. The V<sub>IN</sub> and I<sub>IN</sub> parameters are referenced to V<sub>SS</sub> and are applicable to all six channels. The V<sub>CCUV</sub> parameters are referenced to V<sub>SS</sub>. The V<sub>BSUV</sub> parameters are referenced to V<sub>S</sub>.

Symbol	Description	Min	Typ	Max	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	500	---	---	V	T <sub>J</sub> =25°C, I <sub>LK</sub> =250μA
I <sub>LKH</sub>	Leakage Current of High Side FET's in Parallel		10		μA	T <sub>J</sub> =25°C, V <sub>DS</sub> =500V
I <sub>LKL</sub>	Leakage Current of Low Side FET's in Parallel Plus Gate Drive IC		15		μA	T <sub>J</sub> =25°C, V <sub>DS</sub> =500V
R <sub>DS(ON)</sub>	Drain to Source ON Resistance	---	1.85	2.2	Ω	T <sub>J</sub> =25°C, V <sub>CC</sub> =15V, I <sub>d</sub> = 1A
V <sub>IN,th+</sub>	Positive Going Input Threshold	2.5	---	---	V	
V <sub>IN,th-</sub>	Negative Going Input Threshold	---	---	0.8	V	
V <sub>CCUV+</sub> , V <sub>BBSUV+</sub>	V <sub>CC</sub> and V <sub>BS</sub> Supply Under-Voltage, Positive Going Threshold	8	8.9	9.8	V	
V <sub>CCUV-</sub> , V <sub>BBSUV-</sub>	V <sub>CC</sub> and V <sub>BS</sub> supply Under-Voltage, Negative Going Threshold	7.4	8.2	9	V	
V <sub>CCUVH</sub> , V <sub>BBSUVH</sub>	V <sub>CC</sub> and V <sub>BS</sub> Supply Under-Voltage Lock-Out Hysteresis	---	0.7	---	V	
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current V <sub>IN</sub> =0V	---	---	125	μA	
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> Supply Current V <sub>IN</sub> =0V	---	---	3.35	mA	
I <sub>QCC, ON</sub>	Quiescent V <sub>CC</sub> Supply Current V <sub>IN</sub> =4V	---	---	10	mA	
I <sub>IN+</sub>	Input Bias Current V <sub>IN</sub> =4V	---	100	160	μA	
I <sub>IN-</sub>	Input Bias Current V <sub>IN</sub> =0V	---	--	1	μA	
I <sub>TRIP+</sub>	I <sub>TRIP</sub> Bias Current V <sub>ITRIP</sub> =4V	---	5	40	μA	
I <sub>TRIP-</sub>	I <sub>TRIP</sub> Bias Current V <sub>ITRIP</sub> =0V	---	--	1	μA	
V <sub>IT, TH+</sub>	I <sub>TRIP</sub> Threshold Voltage	0.37	0.46	0.55	V	
V <sub>IT, TH-</sub>	I <sub>TRIP</sub> Threshold Voltage	---	0.4	---	V	

V <sub>IT,HYS</sub>	I <sub>TRIP</sub> Input Hysteresis	---	0.06	---	V	
R <sub>BR</sub>	Internal Bootstrap Equivalent Resistor Value	---	200	---	Ω	T <sub>J</sub> =25°C
V <sub>RCIN,TH</sub>	RCIN Positive Going Threshold	---	8	---	V	
R <sub>ON,FAULT</sub>	FAULT Open-Drain Resistance	---	50	100	Ω	

Note 4: Characterized, not tested at manufacturing

### Dynamic Electrical Characteristics

(V<sub>CC-COM</sub>) = (V<sub>B</sub>-V<sub>S</sub>) = 15 V. T<sub>A</sub> = 25°C unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
T <sub>ON</sub>	Input to Output Propagation Turn-On Delay Time	---	0.7	1.5	μs	I <sub>D</sub> =1mA, V <sup>+</sup> =50V See Fig.2
T <sub>OFF</sub>	Input to Output Propagation Turn-Off Delay Time	---	0.7	1.5	μs	
T <sub>FIL,IN</sub>	Input Filter Time (HIN, LIN)	200	330	---	ns	V <sub>IN</sub> =0 & V <sub>IN</sub> =4V
T <sub>FIL,EN</sub>	Input Filter Time (EN)	100	200	---	ns	V <sub>IN</sub> =0 & V <sub>IN</sub> =4V
T <sub>BLT-ITRIP</sub>	I <sub>TRIP</sub> Blanking Time	100	330		ns	V <sub>IN</sub> =0 & V <sub>IN</sub> =4V, V <sub>I/Trip</sub> =5V
T <sub>FAULT</sub>	I <sub>trip</sub> to Fault	---	600	1000	ns	V <sub>IN</sub> =0 & V <sub>IN</sub> =4V
T <sub>EN</sub>	EN Falling to Switch Turn-Off		700	1000	ns	V <sub>IN</sub> =0 & V <sub>IN</sub> =4V
T <sub>ITRIP</sub>	I <sub>TRIP</sub> to Switch Turn-Off Propagation Delay	---	950	1300	ns	I <sub>D</sub> =1A, V <sup>+</sup> =50V, See Figure 3

### MOSFET Avalanche Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
EAS	Single Pulse Avalanche Energy	---	150	---	mJ	T <sub>J</sub> =25°C, L=93mH, VDD=150V, I <sub>TEST</sub> =1.8A, TO-220 package

### Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
R <sub>th(J-CT)</sub>	Total Thermal Resistance Junction to Case Top	---	27.4	---	°C/W	One device
R <sub>th(J-CB)</sub>	Total Thermal Resistance Junction to Case Bottom	---	2.2	---	°C/W	One device

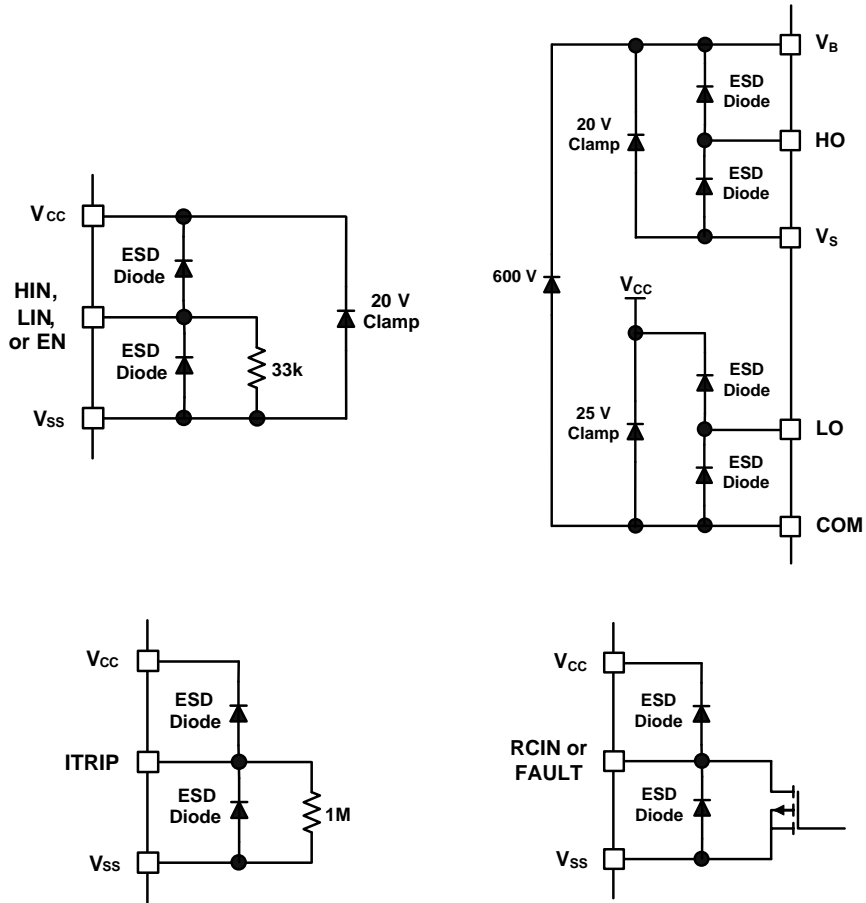
**Qualification Information†**

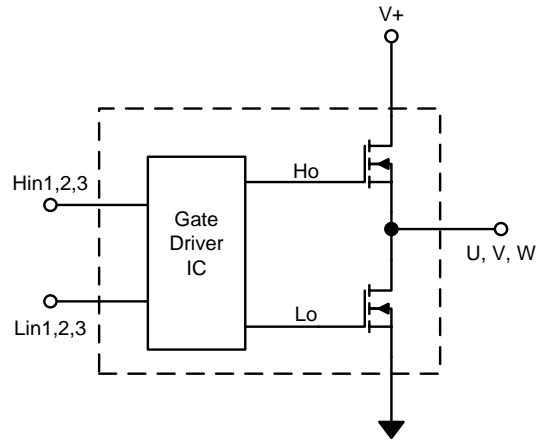
<b>Qualification Level</b>		Industrial <sup>††</sup> (per JEDEC JESD 47E)
<b>Moisture Sensitivity Level</b>		MSL3 <sup>†††</sup> (per IPC/JEDEC J-STD-020C)
<b>ESD</b>	<b>Machine Model</b>	Class B (per JEDEC standard JESD22-A115)
	<b>Human Body Model</b>	Class 2 (per standard ESDA/JEDEC JS-001-2012)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

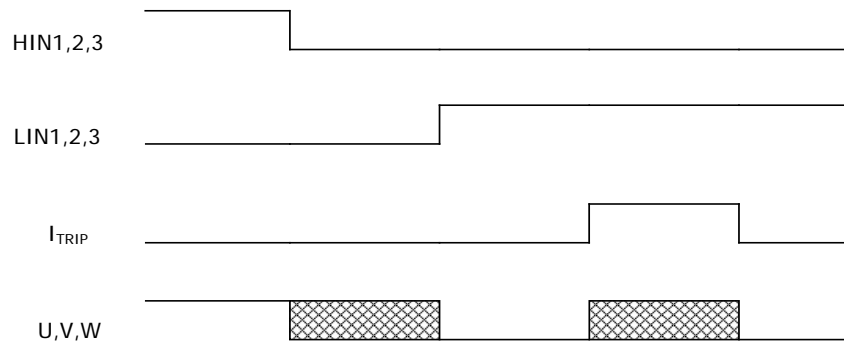
†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

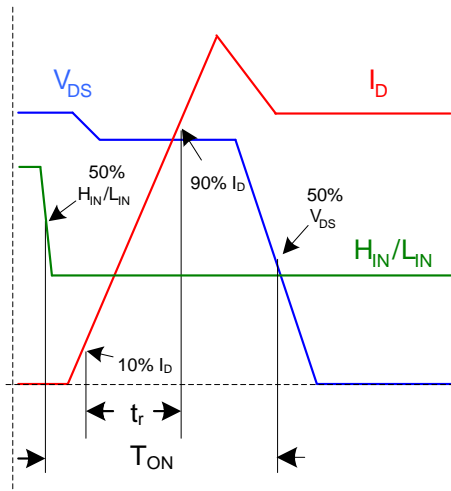
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Input/ Output Pin Equivalent Circuit Diagrams**


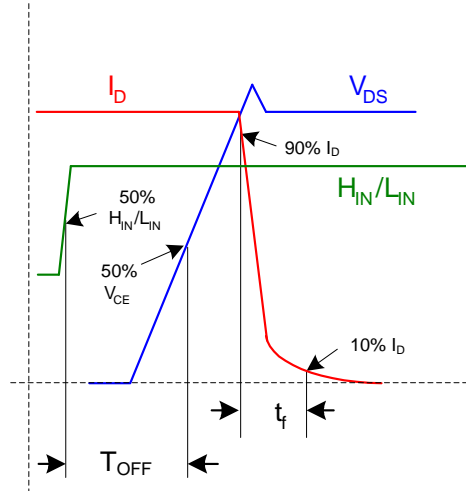
**Input-Output Logic Level Table**


EN	Itrip	Hin1,2,3	Lin1,2,3	U,V,W
1	0	1	0	V+
1	0	0	1	0
1	0	0	0	off
1	1	X	X	off
0	X	X	X	off

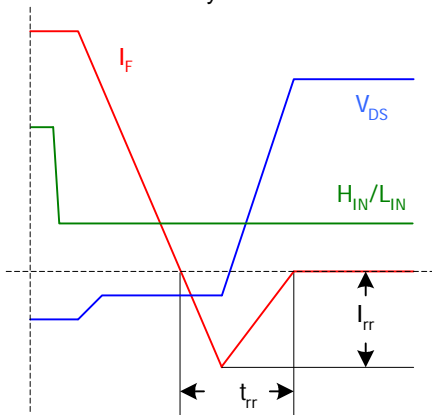

**Figure 1: Input/Output Logic Diagram**



**Figure 2a:** Input to Output propagation turn-on delay time.



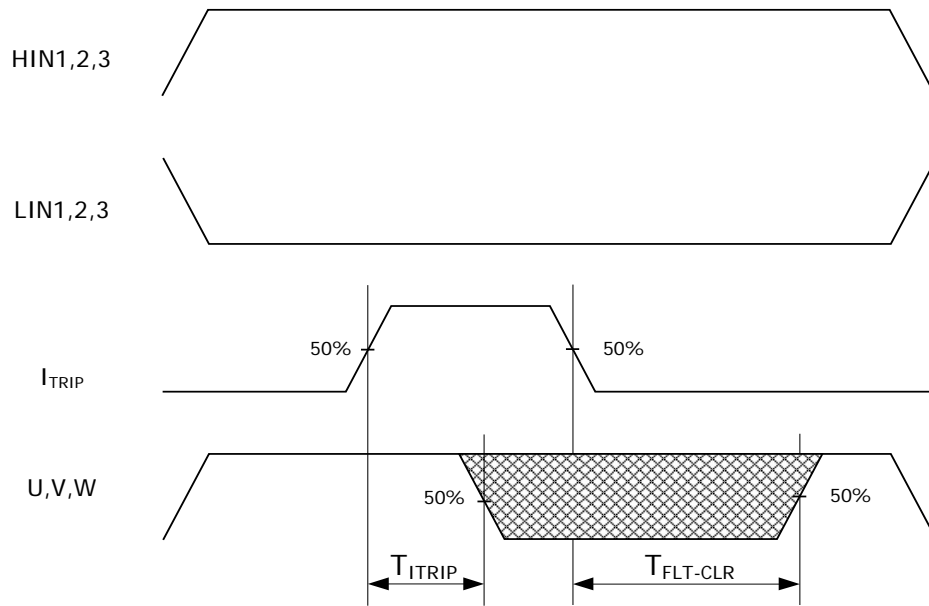
**Figure 2b:** Input to Output propagation turn-off delay time.



**Figure 2c:** Diode Reverse Recovery.

**Figure 2:** Switching Parameter Definitions

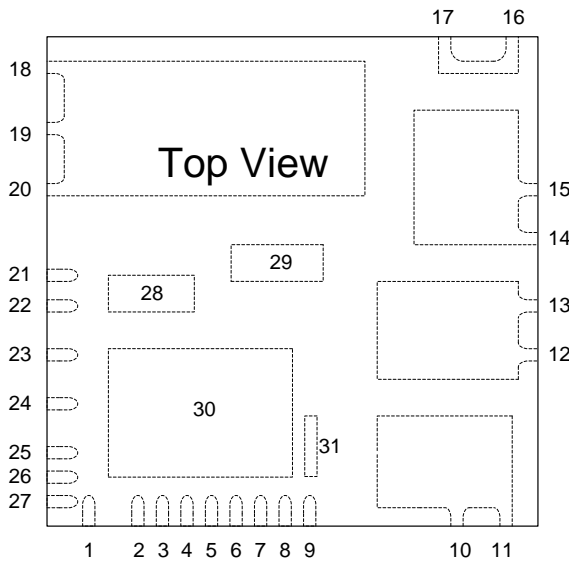




**Figure 3: I<sub>TRIP</sub> Timing Waveform**

**Module Pin-Out Description**

Pin	Name	Description
1	HIN3	Logic Input High Side Gate Driver - Phase 3
2	LIN1	Logic Input Low Side Gate Driver - Phase 1
3	LIN2	Logic Input Low Side Gate Driver - Phase 2
4	LIN3	Logic Input Low Side Gate Driver - Phase 3
5	/FLT	Fault Output
6	I <sub>TRIP</sub>	Current Protection Pin
7	EN	Enable Pin
8	RCIN	RCIN Reset Programming Pin
9	V <sub>SS</sub>	Negative Main Supply
10, 11, 21, 28	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
12, 13, 29	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
14, 15	W,VS3	Output 3 - High Side Floating Supply Offset Voltage
16, 17, 30, 31	V-	Negative Bus Input Voltage, COM
18, 19, 20	V+	Positive Bus Input Voltage
22	VB1	High Side Floating Supply voltage 1
23	VB2	High Side Floating Supply voltage 2
24	VB3	High Side Floating Supply Voltage 3
25	V <sub>CC</sub>	+15V Main Supply
26	HIN1	Logic Input High Side Gate Driver - Phase 1
27	HIN2	Logic Input High Side Gate Driver - Phase 2


**Notes**

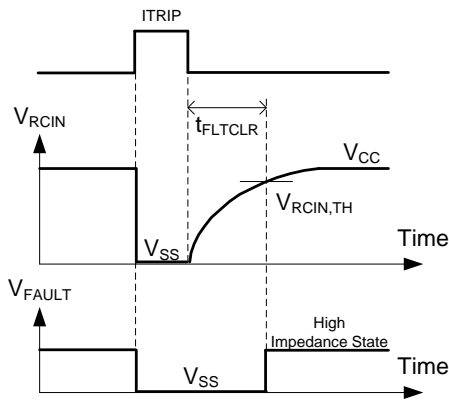
Pin 28,29, 31 are not required to be connected electrically on the PCB

All pins with the same name are internally connected. For example, pins 10, 11, 21 and 28 are internally connected.

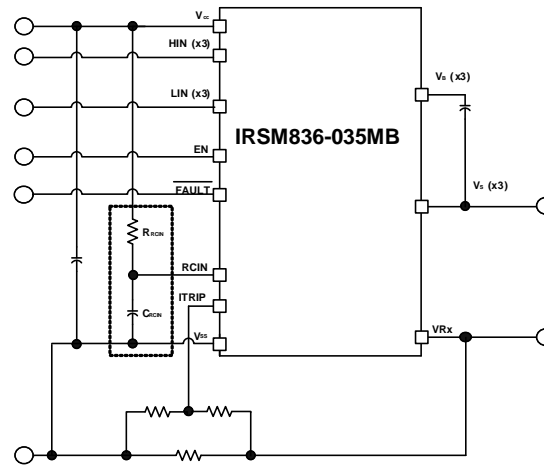
### Fault Reporting and Programmable Fault Clear Timer

The IRSM836-035MB provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the IRSM836-035MB to report a fault via the FAULT pin. The first is an under-voltage condition of  $V_{CC}$  and the second is when the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to  $V_{SS}$  and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to  $V_{CC}$ .

The length of the fault clear time period ( $t_{FLTCLR}$ ) is determined by exponential charging characteristics of the capacitor where the time constant is set by  $R_{RCIN}$  and  $C_{RCIN}$ . In Figure 4 where we see that a fault condition has occurred (UVLO or ITRIP), RCIN and FAULT are pulled to  $V_{SS}$ , and once the fault has been removed, the fault clear timer begins. Figure 5 shows that  $R_{RCIN}$  is connected between the  $V_{CC}$  and the RCIN pin, while  $C_{RCIN}$  is placed between the RCIN and  $V_{SS}$  pins.



**Figure 4:** RCIN and FAULT pin waveforms



**Figure 5:** Programming the fault clear timer

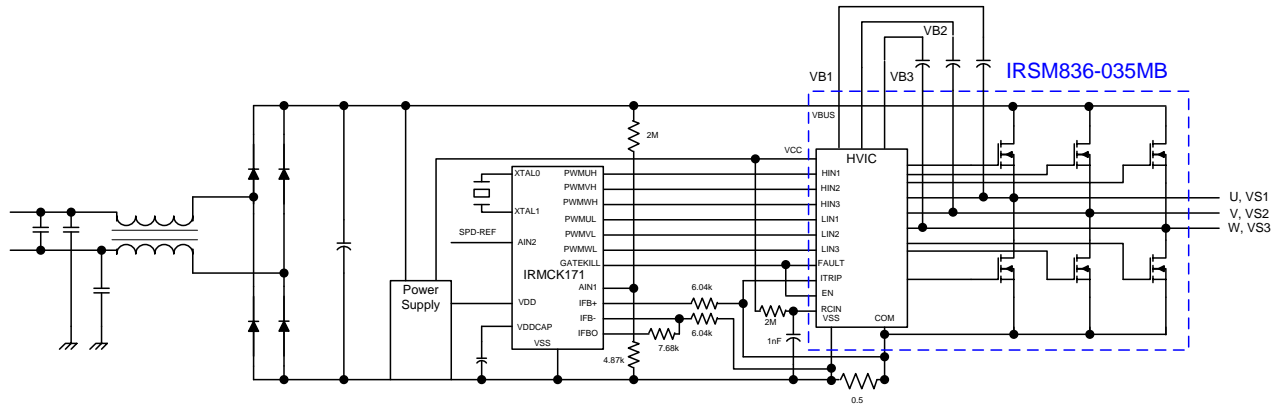
The design guidelines for this network are shown in Table 1.

$C_{RCIN}$	$\leq 1$ nF
	Ceramic
$R_{RCIN}$	0.5 M $\Omega$ to 2 M $\Omega$
	$\gg R_{ON,RCIN}$

**Table 1:** Design guidelines

The length of the fault clear time period can be determined by using the formula below.

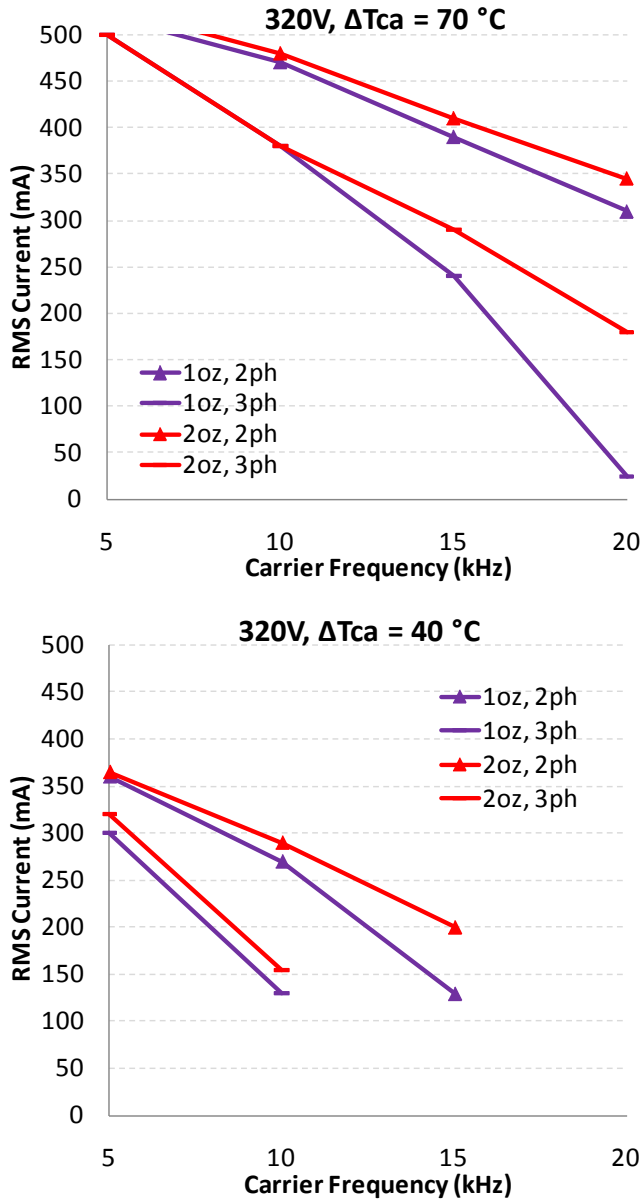
$$t_{FLTCLR} = -(R_{RCIN} C_{RCIN}) \ln \left( 1 - \frac{V_{RCIN,TH}}{V_{CC}} \right)$$

**Typical Application Connection IRSM836-035MB**


1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. In order to provide good decoupling between VCC-VSS and VB1,2,3-VS1,2,3 terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1 $\mu$ F, are recommended.
3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on application note AN-1044.
4. PWM generator must be disabled within Fault duration to guarantee shutdown of the system. Over-current condition must be cleared before resuming operation.

### Current Capability in a Typical Application

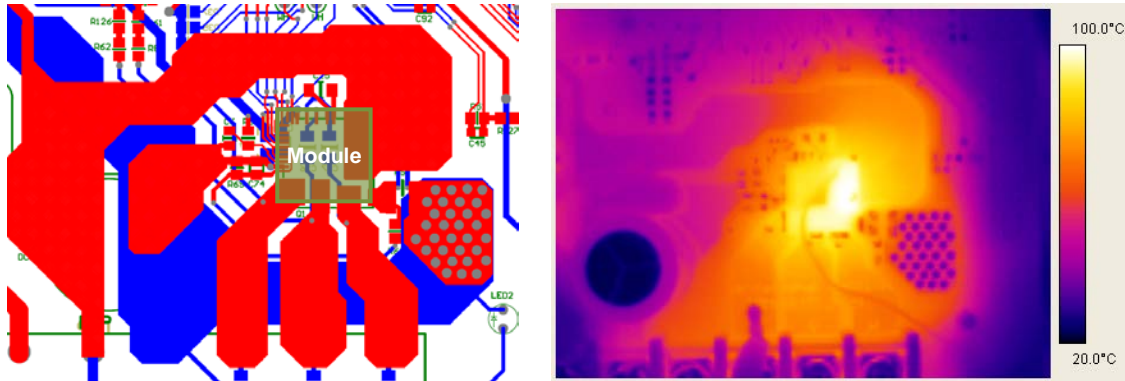
Figure 6 shows the current capability for this module at specified conditions. The current capability of the module is affected by application conditions including the PCB layout, ambient temperature, maximum PCB temperature, modulation scheme, PCB copper thickness and so on. The curves below were obtained from measurements carried out on the IRMCS1171 reference design board which includes the IRSM836-035MB and IR's IRMCK171 digital control IC.



**Figure 6:** Maximum Sinusoidal Phase Current vs. PWM Switching Frequency  
Sinusoidal Modulation,  $V^+ = 320\text{V}$ ,  $\text{PF} = 0.95$

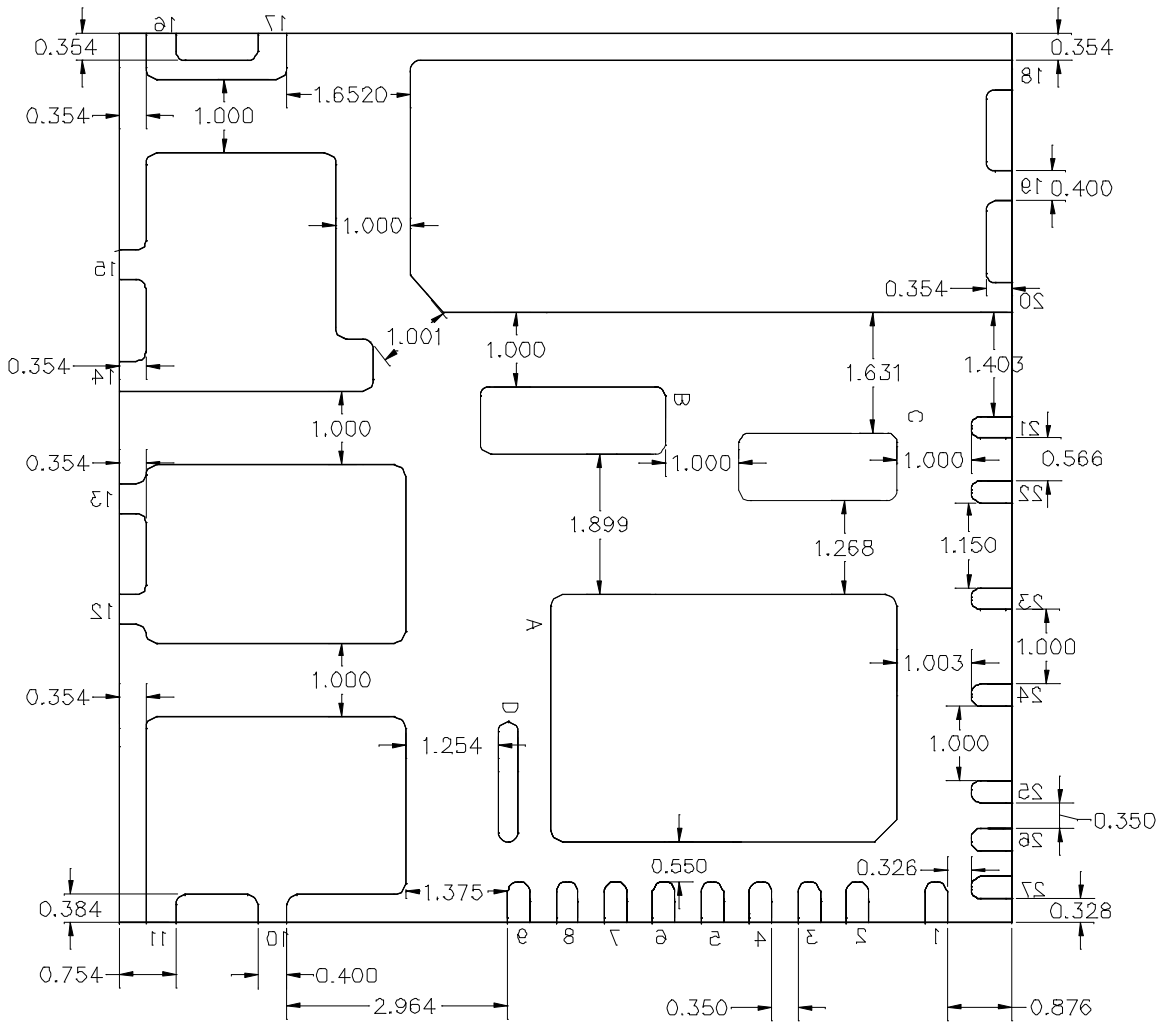
## PCB Example

Figure 7 below shows an example layout for the application PCB. The effective area of the V+ top-layer copper plane is ~3cm<sup>2</sup> in this example. For an FR4 PCB with 1oz copper,  $R_{th(J-A)}$  is about 40°C/W. A lower  $R_{th(J-A)}$  can be achieved using thicker copper and/or additional layers.

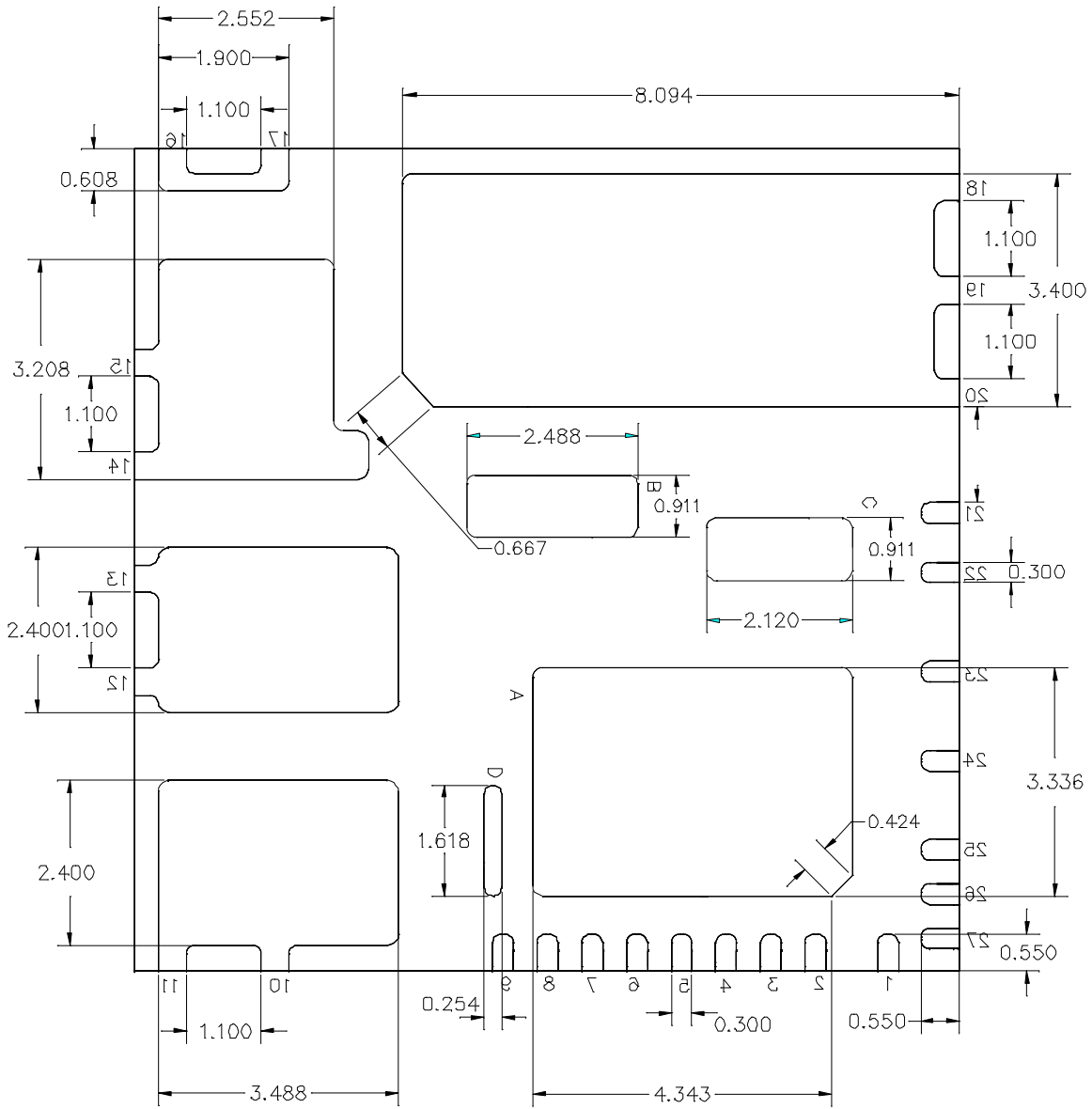


**Figure 7:** PCB layout example and corresponding thermal image

At the module's typical operating conditions,  $dV/dt$  of the phase node voltage is influenced by the load capacitance which includes parasitic capacitance of the PCB, MOSFET output capacitance and motor winding capacitance. To turn off the MOSFET, the load capacitance needs to be charged by the phase current. For the IRMCS1171 reference design, turn-off  $dV/dt$  ranges from 2 to 5 V/ns depending on the phase current magnitude. Turn-on  $dV/dt$  is influenced by PCB parasitic capacitance and motor winding capacitance and typically ranges from 4 to 6 V/ns. The MOSFET turn-on loss combined with the complimentary body diode reverse recovery loss comprises the majority of the total switching losses. Two-phase modulation can be used to reduce switching losses and run the module at higher phase currents.

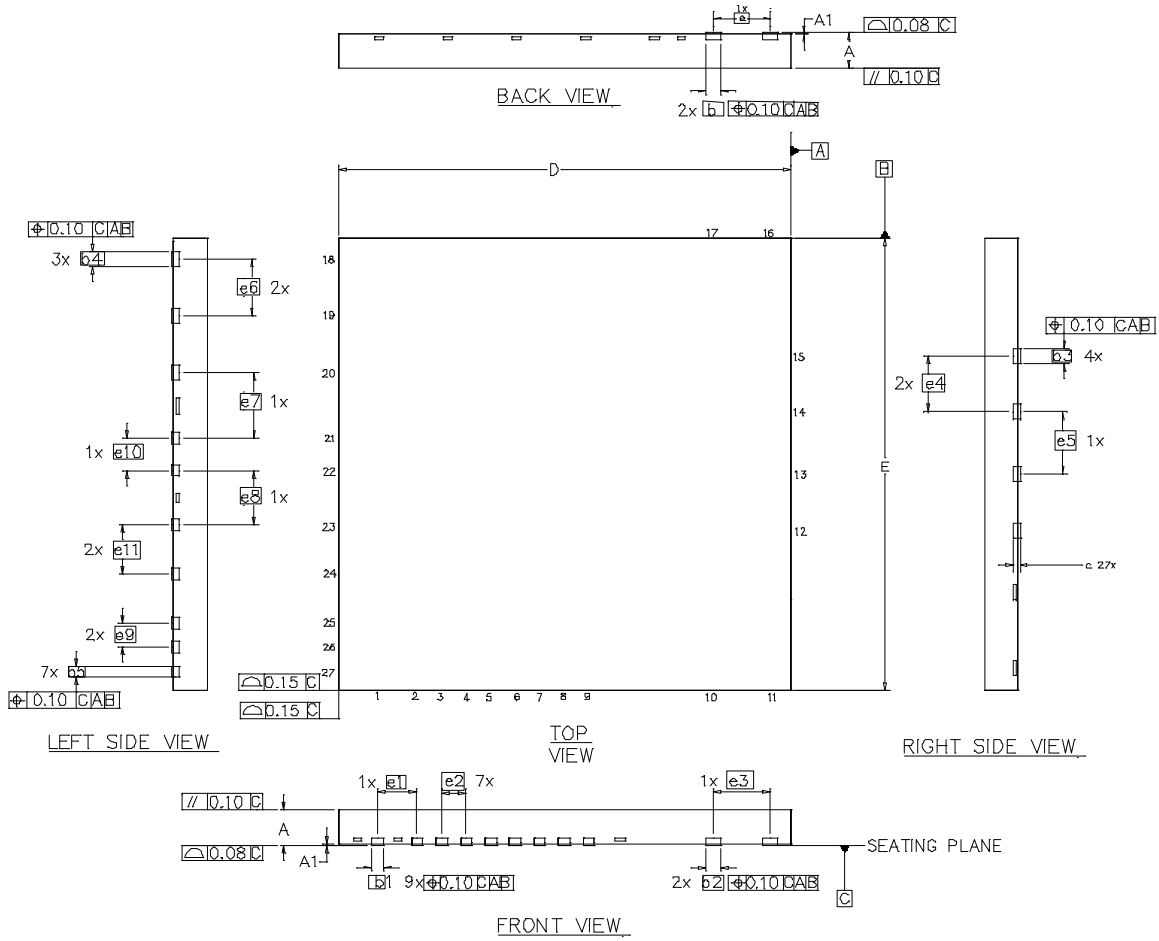
**27L Package Outline IRSM836-035MB (Bottom View)**


Dimensions in mm

**27L Package Outline IRSM836-035MB (Bottom View)**


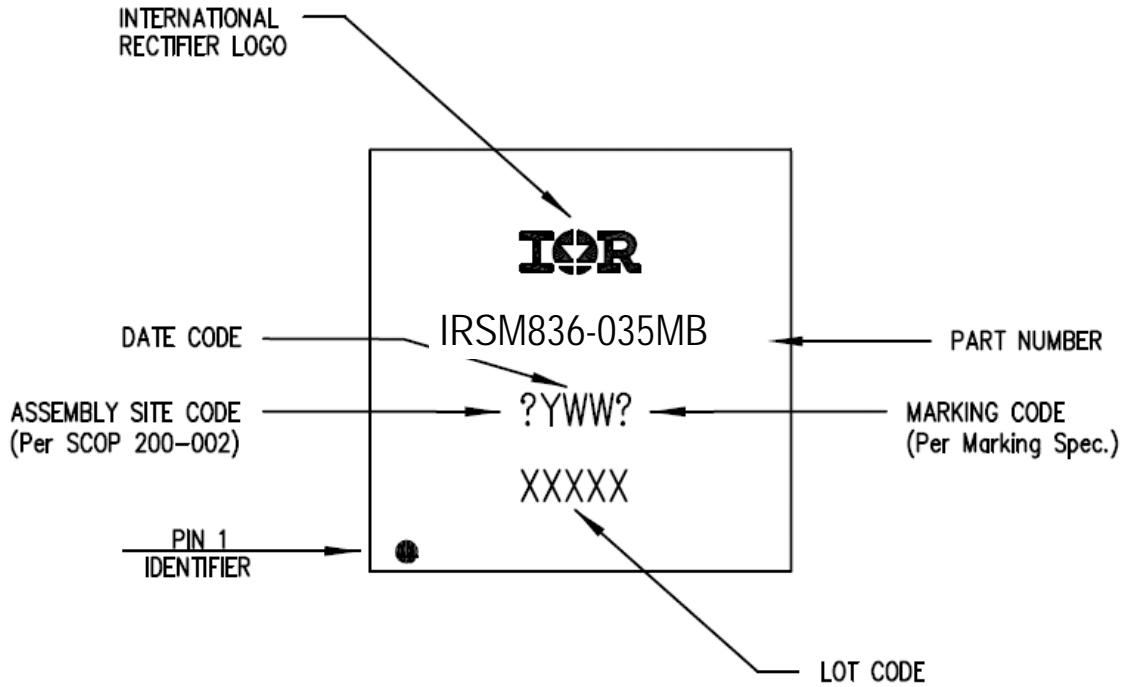
Dimensions in mm



**27L Package Outline IRSM836-035MB (Top and Side View)**


DIM	MILLIMETERS		e	BASIC
	MIN	MAX		
A	0.800	1.000	e1	1.056
A1	0.000	0.050	e2	0.650
b	0.350	0.450	e3	1.500
b1	0.250	0.350	e4	1.500
b2	0.250	0.350	e5	1.650
b3	0.350	0.450	e6	1.500
b4	0.350	0.450	e7	1.753
b5	0.250	0.350	e8	1.450
c	0.203	REF.	e9	0.650
D	12.000	BASIC	e10	0.866
E	12.000	BASIC	e11	1.300

**27L Top Marking**



## Revision History

January 30, 2013      Formatting corrections; added notes about what pins are internally connected; updated ordering table stating all parts are PbF.

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