

## 85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection

### Features

- 5.5V to 16V Gate Drive Supply Voltage Range
- Advanced Adaptive Dead Time
- Intelligent Shoot-Through Protection:
  - MIC4605-1: Dual TTL inputs
  - MIC4605-2: Single PWM input
- Enable Input for On/Off Control
- On-Chip Bootstrap Diode
- Fast 35 ns Propagation Times
- Drives 1000 pF Load with 20 ns Rise and Fall Times
- Low-Power Consumption: 135  $\mu$ A Quiescent Current
- Separate High-Side and Low-Side Undervoltage Protection
- -40°C to +125°C Junction Temperature Range
- AEC-Q100 Qualified for the SOIC Package

### Applications

- Fans
- Power Inverters
- High-Voltage Step-Down Regulators
- Half, Full and 3-Phase Bridge Motor Drives
- Appliances
- E-Bikes
- Automotive Applications

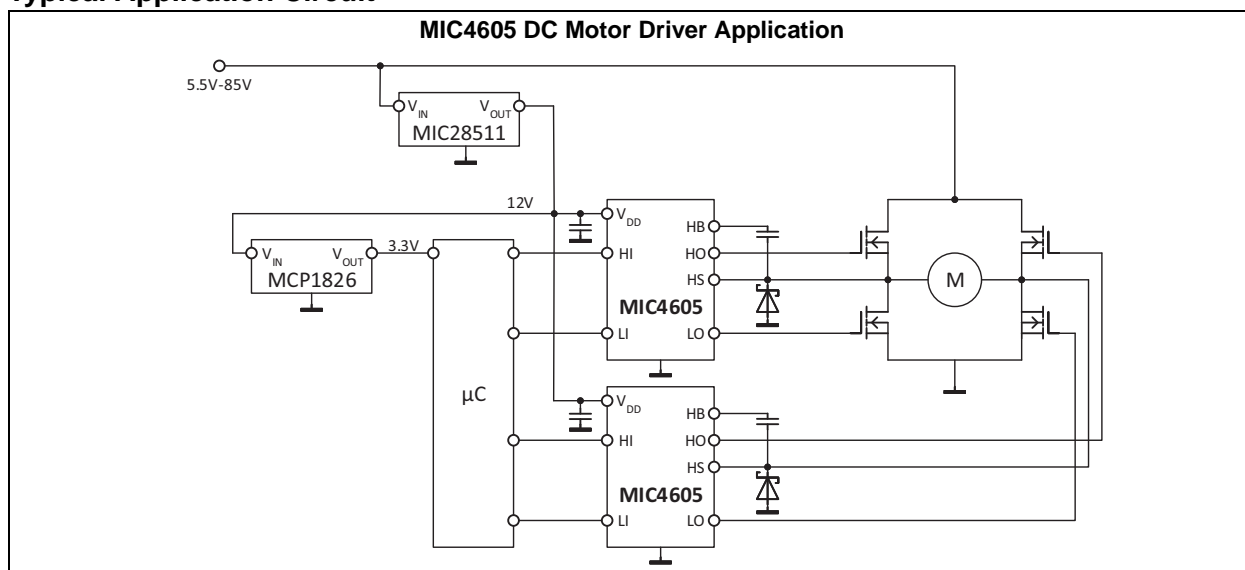
### General Description

The MIC4605 is an 85V half-bridge MOSFET driver that features adaptive dead time and shoot-through protection. The adaptive dead-time circuitry actively monitors the half-bridge outputs to minimize the time between high-side and low-side MOSFET transitions, thus maximizing power efficiency. Shoot-through protection circuitry prevents erroneous inputs and noise from turning both MOSFETs on at the same time.

The MIC4605 also offers a wide 5.5V to 16V operating supply range to maximize system efficiency. The low 5.5V operating voltage allows longer run times in battery-powered applications. Additionally, the MIC4605 device's adjustable gate drive sets the gate drive voltage to  $V_{DD}$  for optimal MOSFET  $R_{DS(ON)}$ , which minimizes power loss due to the MOSFET's  $R_{DS(ON)}$ .

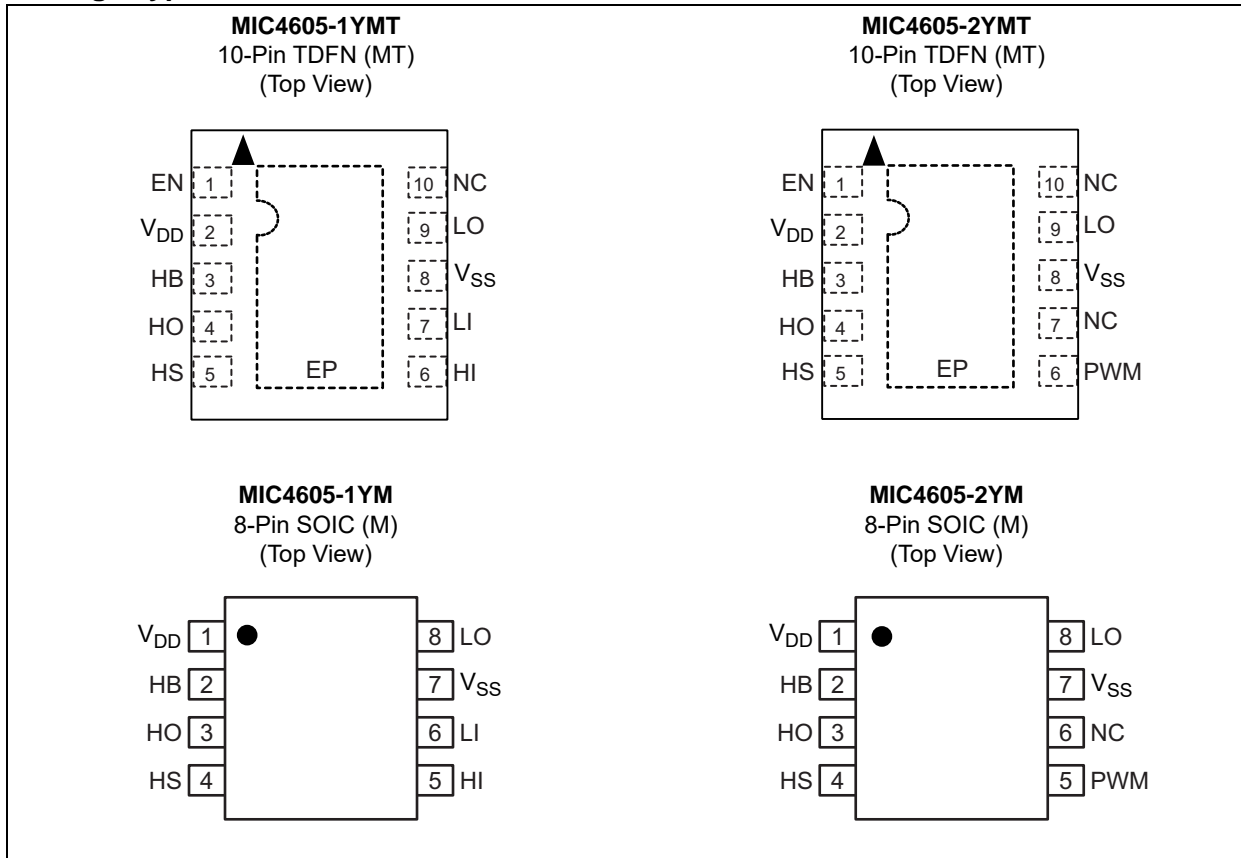
The MIC4605 is available in an 8-pin SOIC package and a tiny 10-pin 2.5 mm x 2.5 mm TDFN package. Both packages have an operating junction temperature range of -40°C to +125°C.

### Typical Application Circuit



# MIC4605

## Package Types



**Note:** See [Table 3-1](#) for pin descriptions.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage ( $V_{DD}$ , $V_{HB} - V_{HS}$ )	-0.3V to +18V
Input Voltages ( $V_{LI}$ , $V_{HI}$ , $V_{EN}$ )	-0.3V to $V_{DD} + 0.3V$
Voltage on LO ( $V_{LO}$ )	-0.3V to $V_{DD} + 0.3V$
Voltage on HO ( $V_{HO}$ )	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on HS (Continuous)	-0.3V to +90V
Voltage on HB	+108V
Average Current in $V_{DD}$ to HB Diode	100 mA
ESD Rating ( <b>Note 1</b> )	HBM: 1 kV; MM: 200V

### Operating Ratings‡

Supply Voltage ( $V_{DD}$ ) [Decreasing $V_{DD}$ ]	+5.25V to +16V
Supply Voltage ( $V_{DD}$ ) [Increasing $V_{DD}$ ]	+5.5V to +16V
Voltage on HS	-0.3V to +85V
Voltage on HS (Repetitive Transient < 5 $\mu$ s)	-2V to +90V
HS Slew Rate	50 V/ns
Voltage on HB	$V_{HS} + V_{DD}$
and/or	$V_{DD} - 1V$ to $V_{DD} + 85V$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ **Notice:** The device is not ensured to function outside its operating ratings.

**Note 1:** Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 k $\Omega$  in series with 100 pF.

**TABLE 1-1: ELECTRICAL CHARACTERISTICS**

<b>Electrical Characteristics:</b> Unless otherwise indicated: $V_{DD} = V_{HB} = 12V$ ; $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO; $T_A = +25^\circ C$ . <b>Bold</b> values indicate $-40^\circ C \leq T_J \leq +125^\circ C$ . <sup>(1)</sup>						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Supply Current</b>						
$V_{DD}$ Quiescent Current	$I_{DD}$	—	100	<b>250</b>	$\mu A$	LI = HI = 0V
$V_{DD}$ Shutdown Current	$I_{DDSH}$	—	2.2	<b>10</b>	$\mu A$	EN = 0V with HS = floating
		—	25	<b>50</b>		EN = 0V
$V_{DD}$ Operating Current	$I_{DDO}$	—	170	<b>500</b>	$\mu A$	f = 20 kHz
Total HB Quiescent Current	$I_{HB}$	—	35	<b>75</b>	$\mu A$	LI = HI = 0V or LI = 0V and HI = 5V
Total HB Operating Current	$I_{HBO}$	—	50	<b>400</b>	$\mu A$	f = 20 kHz
HB to $V_{SS}$ Quiescent Current	$I_{HBS}$	—	0.05	5	$\mu A$	$V_{HS} = V_{HB} = 90V$
HB to $V_{SS}$ Operating Current	$I_{HBSO}$	—	30	<b>300</b>	$\mu A$	f = 20 kHz
<b>Input (TTL: LI, HI, EN) (<b>Note 2</b>)</b>						
Low-Level Input Voltage	$V_{IL}$	—	—	<b>0.8</b>	V	
High-Level Input Voltage	$V_{IH}$	<b>2.2</b>	—	—	V	
Input Voltage Hysteresis	$V_{HYS}$	—	0.1	—	V	

**Note 1:** Specifications are for packaged product only.

- $V_{IL(MAX)}$  = maximum positive voltage applied to the input which will be accepted by the device as a logic low.  
 $V_{IH(MIN)}$  = minimum positive voltage applied to the input which will be accepted by the device as a logic high.
- Not production tested.

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**TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise indicated: $V_{DD} = V_{HB} = 12V$ ; $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO; $T_A = +25^\circ C$ . <b>Bold</b> values indicate $-40^\circ C \leq T_J \leq +125^\circ C$ . <sup>(1)</sup>						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Pull-Down Resistance	$R_I$	<b>100</b>	300	<b>500</b>	k $\Omega$	LI and HI
		<b>50</b>	130	<b>250</b>		PWM
<b>Undervoltage Protection</b>						
$V_{DD}$ Falling Threshold	$V_{DDF}$	<b>4.0</b>	4.4	<b>4.9</b>	V	
$V_{DD}$ Threshold Hysteresis	$V_{DDH}$	—	0.25	—	V	
HB Falling Threshold	$V_{HBF}$	<b>4.0</b>	4.4	<b>4.9</b>	V	
HB Threshold Hysteresis	$V_{HBH}$	—	0.25	—	V	
<b>Bootstrap Diode</b>						
Low-Current Forward Voltage	$V_{DL}$	—	0.4	<b>0.70</b>	V	$I_{V_{DD-HB}} = 100 \mu A$
High-Current Forward Voltage	$V_{DH}$	—	0.7	<b>1.0</b>	V	$I_{V_{DD-HB}} = 50 \text{ mA}$
Dynamic Resistance	$R_D$	—	2.0	<b>5.0</b>	$\Omega$	$I_{V_{DD-HB}} = 50 \text{ mA}$
<b>LO Gate Driver</b>						
Low-Level Output Voltage	$V_{OLL}$	—	0.3	<b>0.6</b>	V	$I_{LO} = 50 \text{ mA}$
High-Level Output Voltage	$V_{OHL}$	—	0.5	<b>1.0</b>	V	$I_{LO} = -50 \text{ mA}$ , $V_{OHL} = V_{DD} - V_{LO}$
Peak Sink Current	$I_{OHL}$	—	1	—	A	$V_{LO} = 0V$ ( <b>Note 3</b> )
Peak Source Current	$I_{OLL}$	—	1	—	A	$V_{LO} = 12V$ ( <b>Note 3</b> )
<b>HO Gate Driver</b>						
Low-Level Output Voltage	$V_{OLH}$	—	0.3	<b>0.6</b>	V	$I_{HO} = 50 \text{ mA}$
High-Level Output Voltage	$V_{OHH}$	—	0.5	<b>1.0</b>	V	$I_{HO} = -50 \text{ mA}$ , $V_{OHH} = V_{HB} - V_{HO}$
Peak Sink Current	$I_{OHH}$	—	1	—	A	$V_{HO} = 0V$ ( <b>Note 3</b> )
Peak Source Current	$I_{OLH}$	—	1	—	A	$V_{HO} = 12V$ ( <b>Note 3</b> )
<b>Switching Specifications (LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high)</b>						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	$t_{LPHL}$	—	35	<b>75</b>	ns	
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	$t_{HPHL}$	—	35	<b>75</b>	ns	
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	$t_{LPLH}$	—	35	<b>75</b>	ns	
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	$t_{HPLH}$	—	35	<b>75</b>	ns	
Output Rise/Fall Time	$t_{RC/FC}$	—	20	—	ns	$C_L = 1000 \text{ pF}$
Output Rise/Fall Time (3V to 9V)	$t_{R/F}$	—	0.8	—	$\mu s$	$C_L = 0.1 \mu F$ ( <b>Note 3</b> )
Minimum Input Pulse Width that Changes the Output	$t_{PW}$	—	50	—	ns	<b>Notes 2, 3</b>

**Note 1:** Specifications are for packaged product only.

- 2:**  $V_{IL(MAX)}$  = maximum positive voltage applied to the input which will be accepted by the device as a logic low.  
 $V_{IH(MIN)}$  = minimum positive voltage applied to the input which will be accepted by the device as a logic high.
- 3:** Not production tested.

**TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise indicated: $V_{DD} = V_{HB} = 12V$ ; $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO; $T_A = +25^\circ C$ . <b>Bold</b> values indicate $-40^\circ C \leq T_J \leq +125^\circ C$ . <sup>(1)</sup>						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Switching Specifications: PWM Mode (MIC4605-2) or LI/Hi Mode (MIC4605-1) with Overlapping LI/Hi Inputs</b>						
Delay from PWM Going High/LI Low to LO Going Low	$t_{LOOFF}$	—	35	<b>75</b>	ns	
LO Output Voltage Threshold for LO FET to be Considered Off	$V_{LOOFF}$	—	1.9	—	V	Note 3
Delay from LO Off to HO Going High	$t_{HOON}$	—	35	<b>75</b>	ns	
Delay from PWM Going Low/Hi Low to HO Going Low	$t_{HOOFF}$	—	35	<b>75</b>	ns	
Switch Node Voltage Threshold Signaling HO is Off	$V_{SWTH}$	1	2.2	4	V	
<b>Switching Specifications: PWM Mode (MIC4605-2) or LI/Hi Mode (MIC4605-1) with Overlapping LI/Hi Inputs</b>						
Delay Between HO FET Being Considered Off to LO Turning On	$t_{LOON}$	—	35	<b>75</b>	ns	
For HS Low/LI High, Delay from PWM/Hi Low to LO Going HI	$t_{LOONHI}$	—	80	<b>150</b>	ns	
Force LO On if $V_{SWTH}$ is Not Detected	$t_{SWTO}$	<b>100</b>	250	<b>500</b>	ns	

**Note 1:** Specifications are for packaged product only.

**2:**  $V_{IL(MAX)}$  = maximum positive voltage applied to the input which will be accepted by the device as a logic low.  
 $V_{IH(MIN)}$  = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

**3:** Not production tested.

## TEMPERATURE SPECIFICATIONS<sup>(1)</sup>

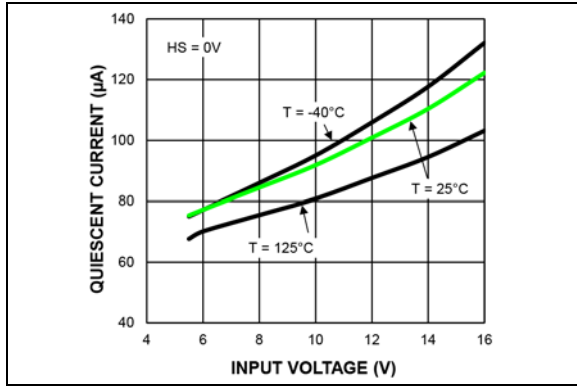
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Junction Operating Temperature Range	$T_J$	-40	—	+125	$^\circ C$	
Storage Temperature Range	$T_S$	-60	—	+150	$^\circ C$	
<b>Package Thermal Resistances</b>						
Thermal Resistance 10-Lead TDFN	$\theta_{JA}$	—	71.4	—	$^\circ C/W$	
Thermal Resistance 8-Lead SOIC	$\theta_{JA}$	—	99	—	$^\circ C/W$	

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125 $^\circ C$  rating. Sustained junction temperatures above +125 $^\circ C$  can impact the device reliability.

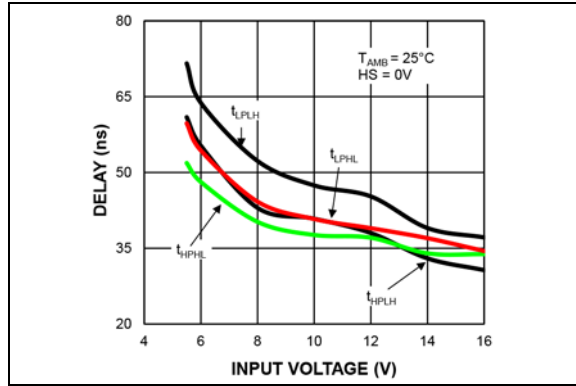
# MIC4605

## 2.0 TYPICAL PERFORMANCE CURVES

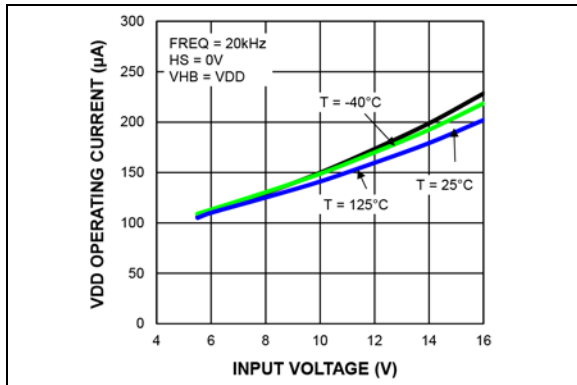
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



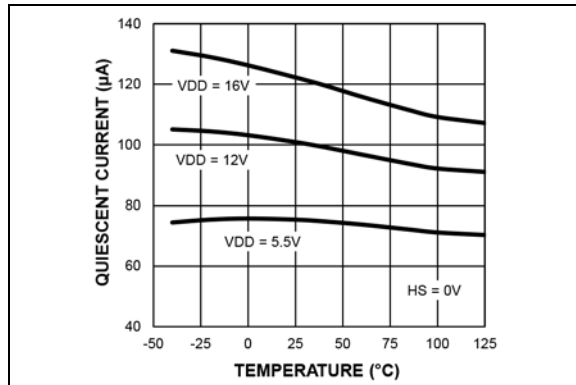
**FIGURE 2-1:** Quiescent Current vs. Input Voltage.



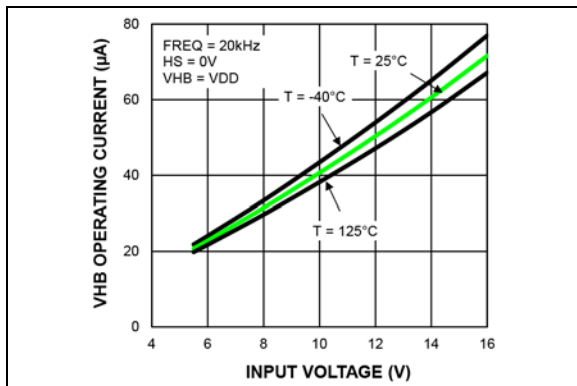
**FIGURE 2-4:** Propagation Delay vs. Input Voltage.



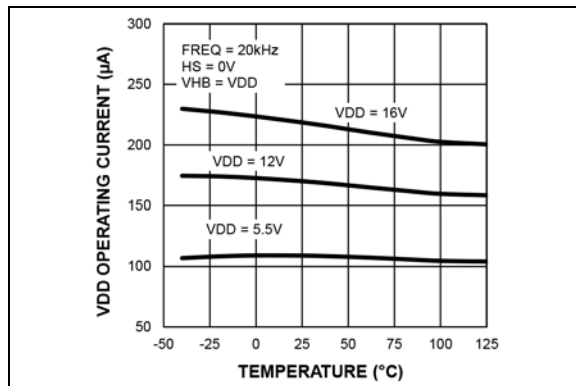
**FIGURE 2-2:**  $V_{DD}$  Operating Current vs. Input Voltage.



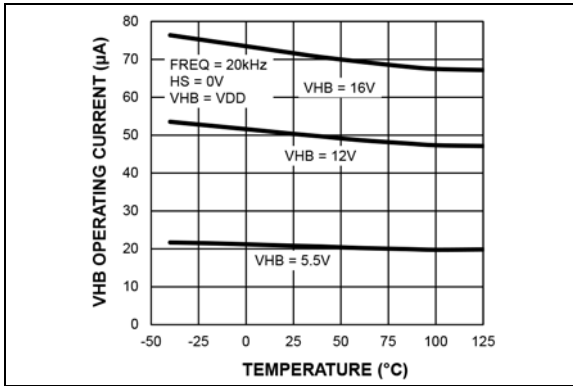
**FIGURE 2-5:** Quiescent Current vs. Temperature.



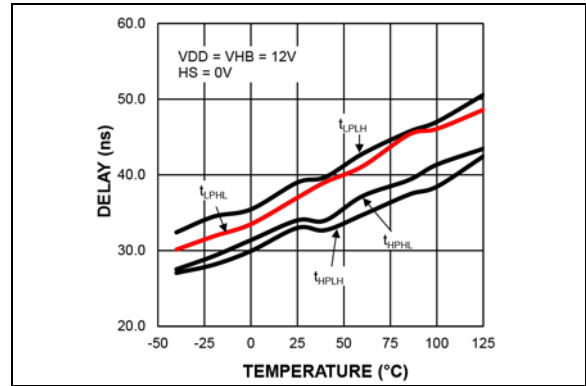
**FIGURE 2-3:**  $V_{HB}$  Operating Current vs. Input Voltage.



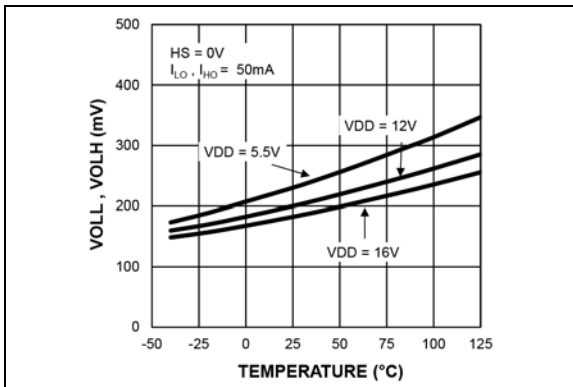
**FIGURE 2-6:**  $V_{DD}$  Operating Current vs. Temperature.



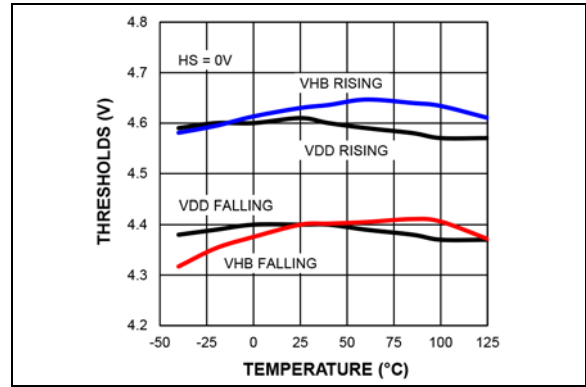
**FIGURE 2-7:**  $V_{HB}$  Operating Current vs. Temperature.



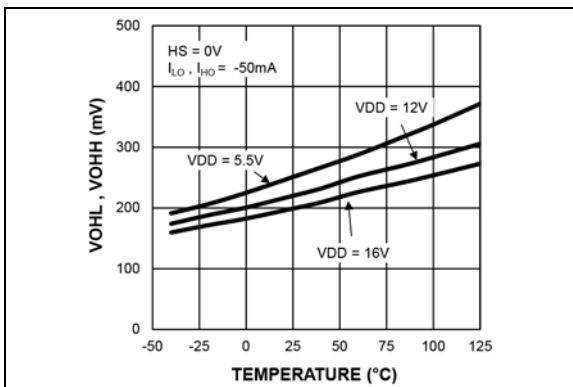
**FIGURE 2-10:** Propagation Delay vs. Temperature.



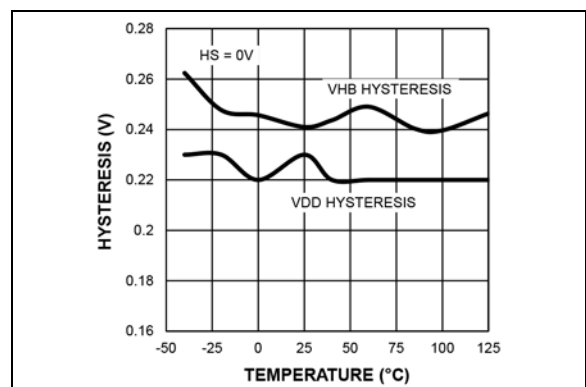
**FIGURE 2-8:** Low-Level Output Voltage vs. Temperature.



**FIGURE 2-11:** UVLO Thresholds vs. Temperature.

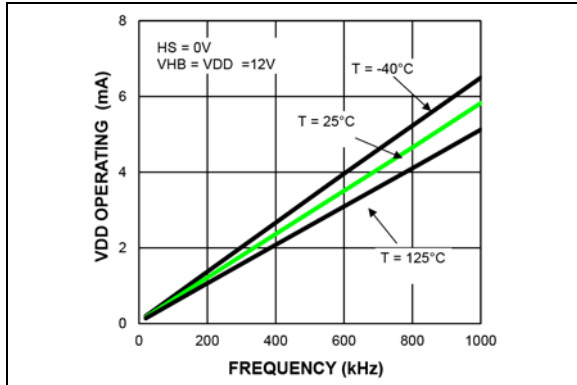


**FIGURE 2-9:** High-Level Output Voltage vs. Temperature.

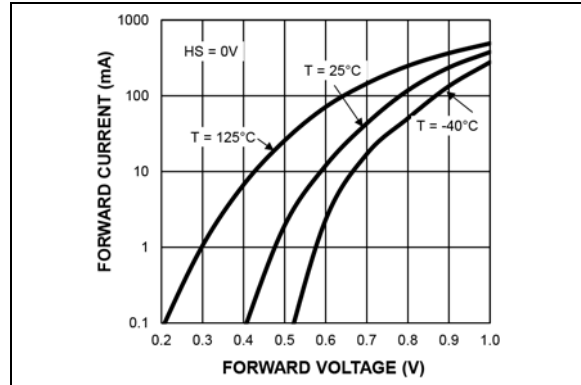


**FIGURE 2-12:** UVLO Hysteresis vs. Temperature.

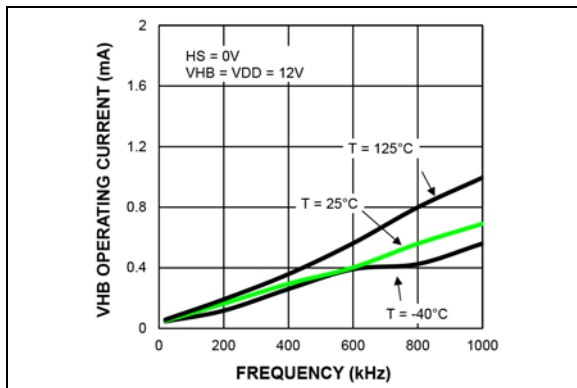
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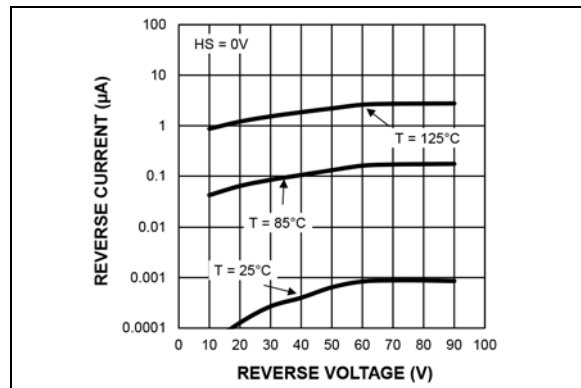
**FIGURE 2-13:**  $V_{DD}$  Operating Current vs. Frequency.



**FIGURE 2-15:** Bootstrap Diode I-V Characteristics.



**FIGURE 2-14:**  $V_{HB}$  Operating Current vs. Frequency.



**FIGURE 2-16:** Bootstrap Diode Reverse Current.



## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

Pin Number MIC4605-1 TDFN	Pin Number MIC4605-2 TDFN	Pin Number MIC4605-1 SOIC	Pin Number MIC4605-2 SOIC	Pin Name	Description
1	1	—	—	EN	Enable Input. Logic high on the enable pin results in normal operation; conversely, the device enters Shutdown mode with a logic low applied to enable.
2	2	1	1	V <sub>DD</sub>	Input Supply for Gate Drivers. Decouple this pin to V <sub>SS</sub> with a > 0.1 μF capacitor.
3	3	2	2	HB	High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and HS. An on-board bootstrap diode is connected from V <sub>DD</sub> to HB.
4	4	3	3	HO	High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
5	5	4	4	HS	High-Side Drive Reference Connection. Connect to source of the external high-side power MOSFET. Connect the bottom of bootstrap capacitor to this pin.
6	—	5	—	HI	High-Side Drive Input.
—	6	—	5	PWM	Single PWM Input. Drives both the high-side and low-side outputs out of phase.
7	—	6	—	LI	Low-Side Drive Input.
—	7	—	6	NC	No Connect. This pin is not connected internally.
8	8	7	7	V <sub>SS</sub>	Driver Reference Supply Input. Generally connected to the power ground of external circuitry.
9	9	8	8	LO	Low-Side Drive Output. Connect to the gate of the external low-side power MOSFET.
10	10	—	—	NC	No Connect. This pin is not connected internally.
EP	EP	—	—	ePAD	Exposed Pad. Connect to V <sub>SS</sub> .

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## 4.0 TIMING DIAGRAMS

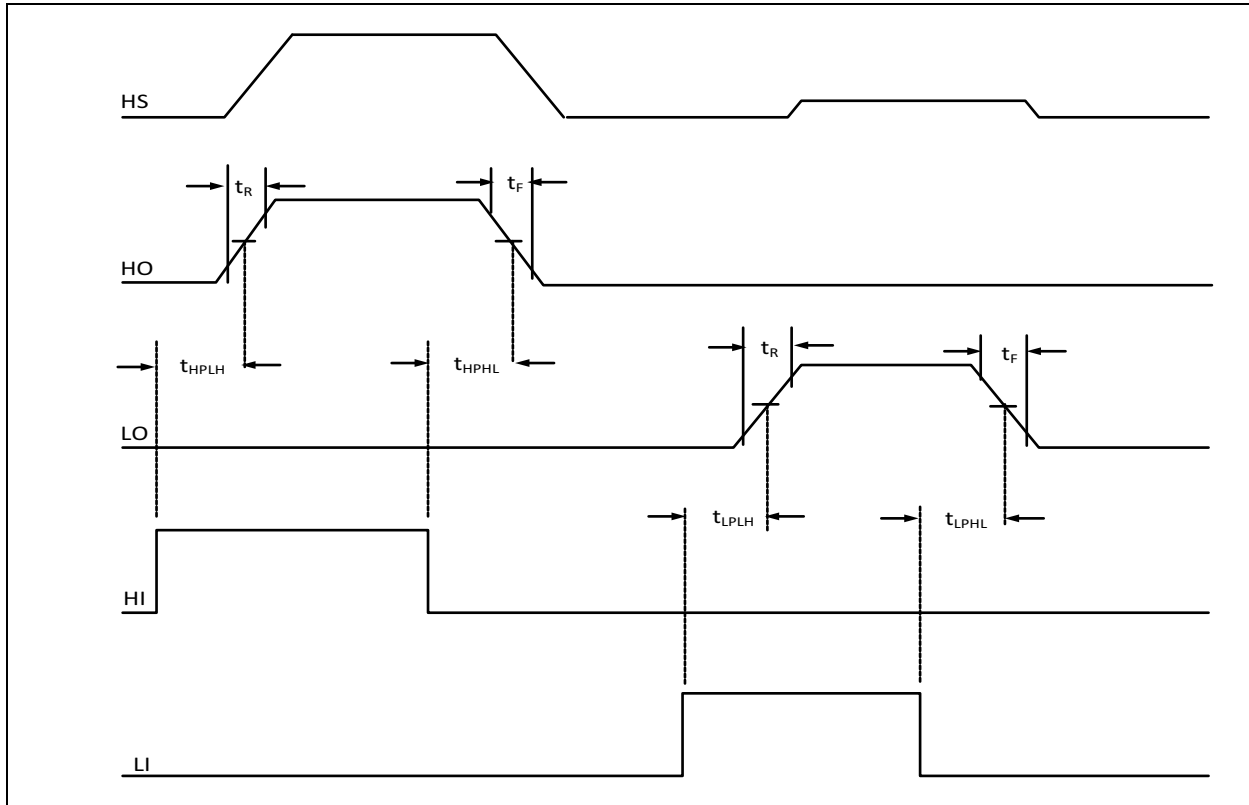
In LI/HI Input mode, the external LI/HI inputs are delayed to the point that HS is low before LI is pulled high and similarly, LO is low before HI goes high.

HO goes high with a high signal on HI after a typical delay of 35 ns ( $t_{HPLH}$ ). HI going low drives HO low, also with a typical delay of 35 ns ( $t_{HPLH}$ ).

Likewise, LI going high forces LO high after a typical delay of 35 ns ( $t_{LPLH}$ ) and LO follows the low transition of LI after a typical delay of 35 ns ( $t_{LPHL}$ ).

HO and LO output rise and fall times ( $t_R/t_F$ ) are typically 20 ns, driving 1000 pF capacitive loads.

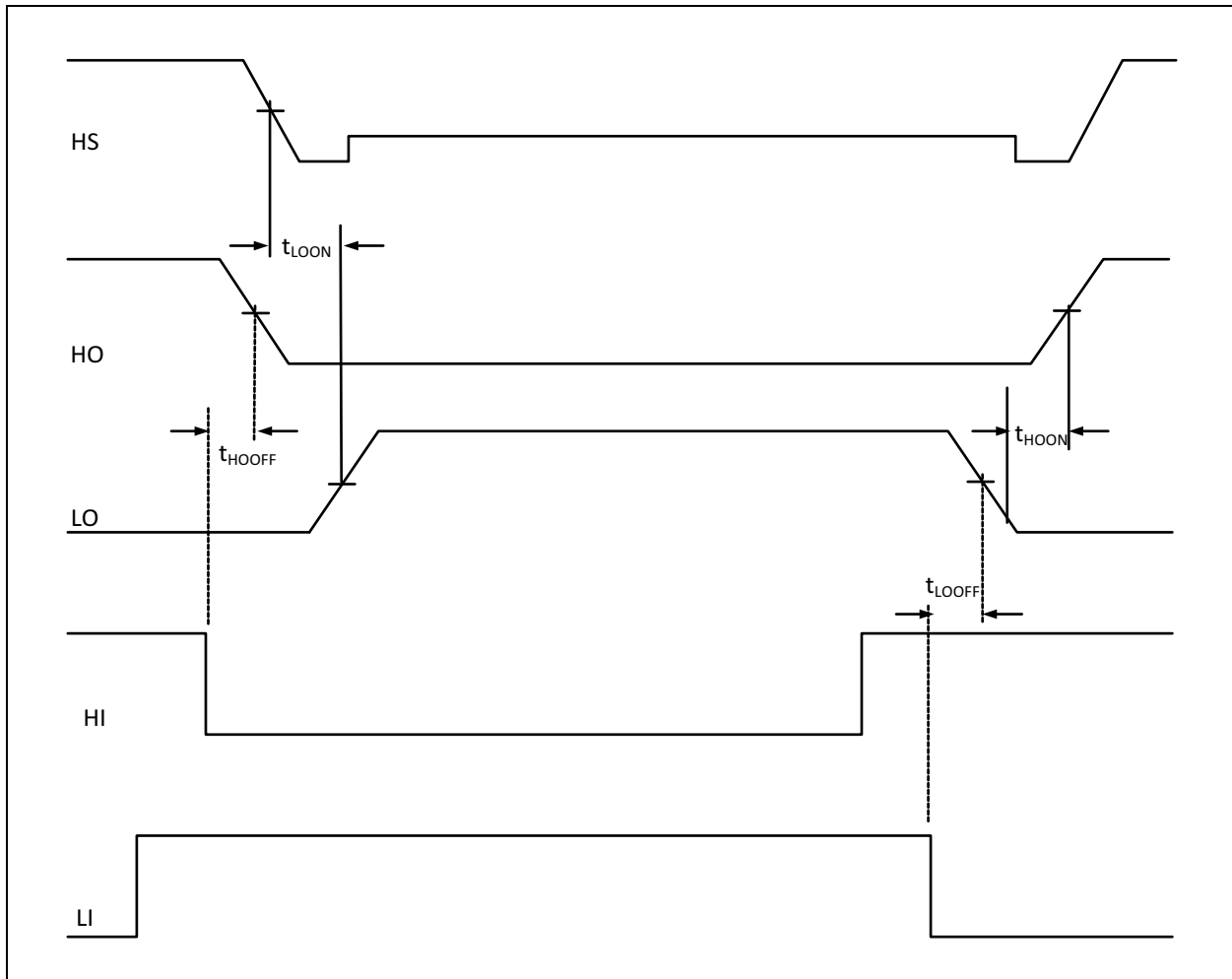
**Note:** All propagation delays are measured from the 50% voltage level.



**FIGURE 4-1:** Separate Non-Overlapping LI/HI Input Mode (MIC4605-1).

When the LI/Hi input on conditions overlap, LO/HO output states are dominated by the first output to be turned on. That is, if LI goes high (on) while HO is high, HO stays high until HI goes low; at which point, after a delay of  $t_{HOFF}$  and when  $HS < 2.2V$ , LO goes high with a delay of  $t_{LOON}$ . Should HS never trip the aforementioned internal comparator reference (2.2V), a falling HI edge delayed by 250 ns will set the "HS latch", allowing LO to go high.

If HS falls very fast, LO will be held low by a 35 ns delay gated by HI going low. Conversely, HI going high (on) when LO is high has no effect on the outputs until LI is pulled low (off) and LO falls to  $< 1.9V$ . Delay from LI going low to LO falling is  $t_{LOFF}$  and delay from LO  $< 1.9V$  to HO being on is  $t_{HOON}$ .



**FIGURE 4-2:** Separate Overlapping LI/Hi Input Mode (MIC4605-1).

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The PWM signal applied to the MIC4605-2 going low causes HO to go low, typically 35 ns ( $t_{HOFF}$ ) after the PWM input goes low; at which point, the switch node HS falls (1-2 in [Figure 4-3](#)).

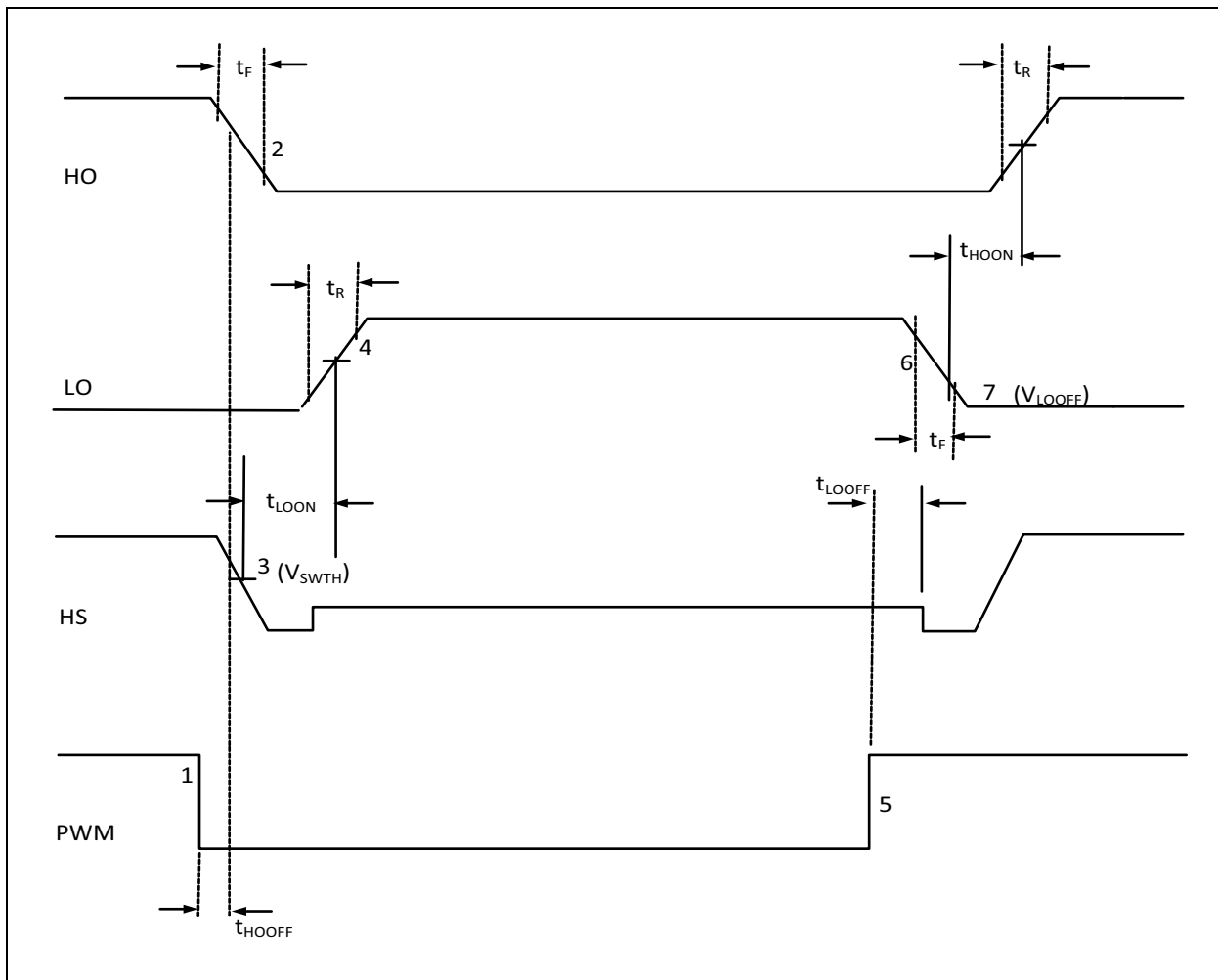
When HS reaches 2.2V ( $V_{SWTH}$ ), the external high-side MOSFET is deemed off and LO goes high, typically within 35 ns ( $t_{LOON}$ ). HS falling below 1.9V sets a latch that can only be reset by PWM going high. This design prevents ringing on HS from causing an indeterminate LO state. Should HS never trip the aforementioned internal comparator reference (2.2V), a falling PWM edge delayed by 250 ns will set the “HS latch”, allowing LO to go high. An 80 ns delay, gated by PWM going low, may determine the time to LO going high for fast falling HS designs (3-4 in [Figure 4-3](#)).

PWM goes high forcing LO low in typically 35 ns ( $t_{LOOFF}$ ) (5-6 in [Figure 4-3](#)).

When LO reaches 1.9V ( $V_{LOOFF}$ ), the low-side MOSFET is deemed off and HO is allowed to go high. The delay between these two points is typically 35 ns ( $t_{LOON}$ ). HO goes high with a high signal on HI after a typical delay of 35 ns ( $t_{HPLH}$ ). HI going low drives HO low, also with a typical delay of 35 ns ( $t_{HPLH}$ ) (7-8 in [Figure 4-3](#)).

HO and LO output rise and fall times ( $t_R/t_F$ ) are typically 20 ns, driving 1000 pF capacitive loads.

**Note:** All propagation delays are measured from the 50% voltage level.



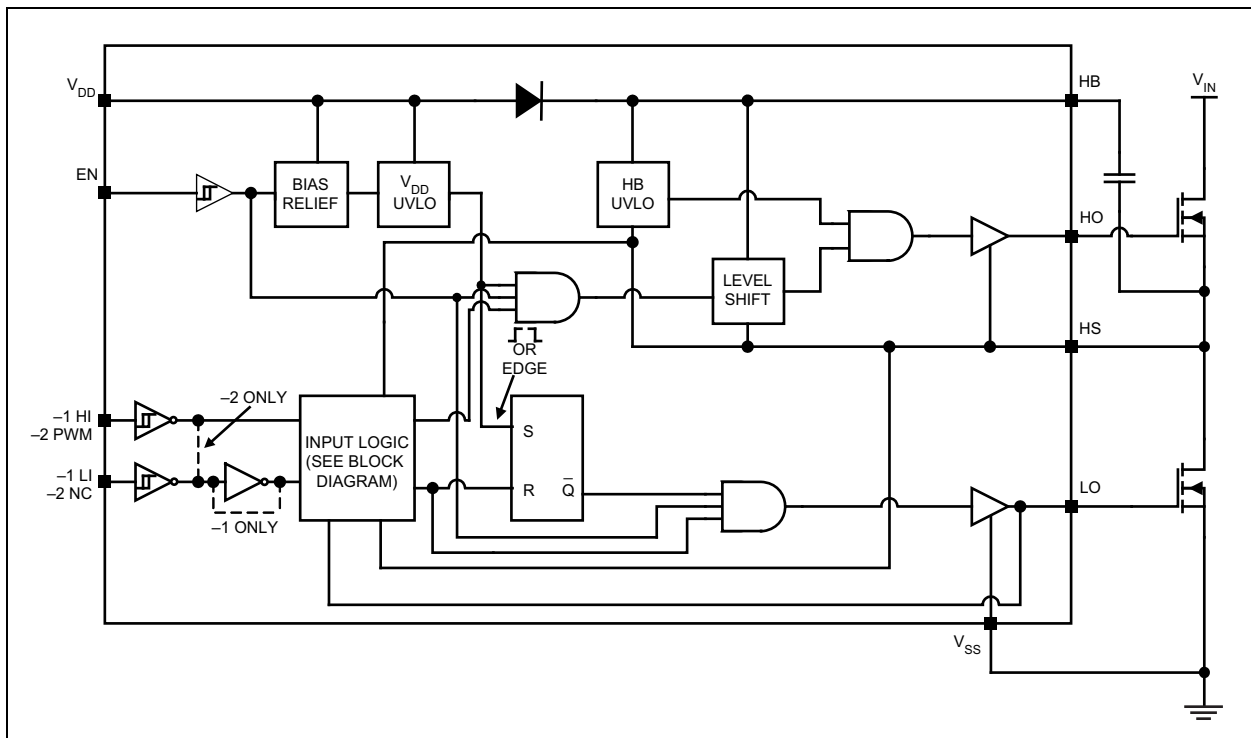
**FIGURE 4-3:** PWM Mode (MIC4605-2).

## 5.0 BLOCK DIAGRAM

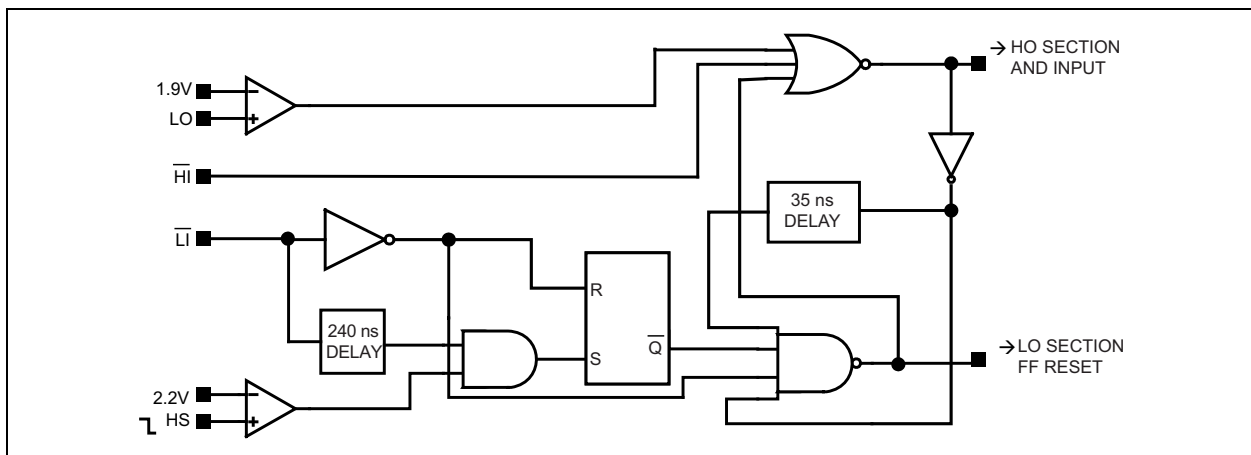
For HO to be high, HI must be high and LO must be low. HO going high is delayed by LO falling below 1.9V. The HI and LI inputs must not rise at the same time to prevent a glitch from occurring on the output. A minimum 50 ns delay between both inputs is recommended.

LO is turned off very quickly on the LI falling edge. LO going high is delayed by the longer of a 35 ns delay of the HO control signal going "off" or the RS latch being set.

The latch is set by the quicker of either the falling edge of HS or the LI gated delay of 240 ns. The latch is present to lockout LO bounce due to ringing on HS. If HS never adequately falls due to the absence of or the presence of a very weak external pull-down on HS, the gated delay of 240 ns at LI will set the latch, allowing LO to transition high. This, in turn, allows the LI start-up pulse to charge the bootstrap capacitor if the load inductor current is very low and HS is uncontrolled. The latch is reset by the LI falling edge.



**FIGURE 5-1:** MIC4605 Top-Level Block Diagram.



**FIGURE 5-2:** MIC4605-1 Cross-Conduction Lockout/PWM Input Logic Block Diagram.

# MIC4605

## 6.0 FUNCTIONAL DESCRIPTION

The MIC4605 is a noninverting, 85V half-bridge MOSFET driver designed to independently drive both high-side and low-side N-channel MOSFETs. The MIC4605 offers a wide 5.5V to 16V operating supply range with either dual TTL inputs (MIC4605-1) or a single PWM input (MIC4605-2). Refer to [Figure 5-1](#).

Both drivers contain an input buffer with hysteresis, a UVLO circuit and an output buffer. The high-side output buffer includes a high-speed level-shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

### 6.1 Start-up and UVLO

The UVLO circuit forces the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the  $V_{DD}$  and  $V_{SS}$  pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

### 6.2 Enable Input

The 10-pin 2.5 mm x 2.5 mm TDFN package features an enable pin for on/off control of the device. Logic high on the enable pin (EN) allows for start-up and normal operation to occur. Conversely, when a logic low is applied on the enable pin, the device enters Shutdown mode.

The start-up time until normal operation after the rising edge of the enable pin (EN) is approximately 100  $\mu$ s. As soon as the device enters Normal Operation mode, the high-side output pin (HO) takes the status according to the input pin (HI for the -1 option or PWM for the -2 option). Entering Normal Operation mode for low side, the LO pin only first gets active after a falling edge of the input pin (LI or PWM).

### 6.3 Input Stage

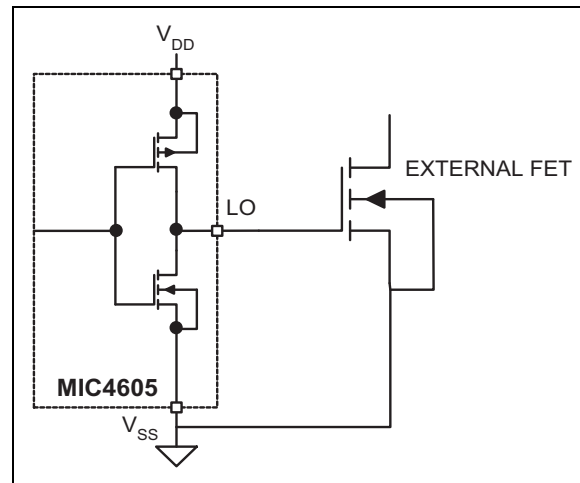
Both the HI/LI pins of the MIC4605-1 and the single PWM input of the MIC4605-2 are referenced to the  $V_{SS}$  pin. The voltage state of the input signal(s) does not change the quiescent current draw of the driver.

The MIC4605 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the  $V_{DD}$  supply voltage and there is no dependence between  $I_{VDD}$  and the input signal amplitude with the MIC4605. This feature makes the MIC4605 an excellent level translator that will drive high-threshold MOSFETs from a low-voltage PWM IC.

## 6.4 Low-Side Driver

A block diagram of the low-side driver is shown in [Figure 6-1](#). The low-side driver is designed to drive a ground ( $V_{SS}$  pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low  $R_{DS(ON)}$  from the external MOSFET.

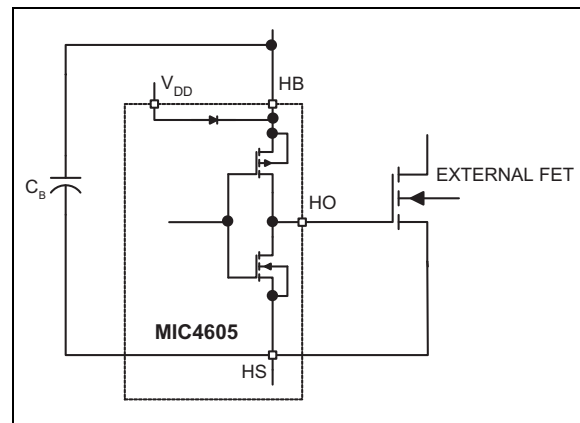
A high level applied to the LI pin causes the upper driver MOSFET to turn on and  $V_{DD}$  voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low-side driver to ground the gate of the external MOSFET.



**FIGURE 6-1:** Low-Side Driver Block Diagram.

## 6.5 High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in [Figure 6-2](#). This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.



**FIGURE 6-2:** High-Side Driver and Bootstrap Circuit Block Diagram.



# MIC4605

## 7.0 APPLICATION INFORMATION

### 7.1 Adaptive Dead Time

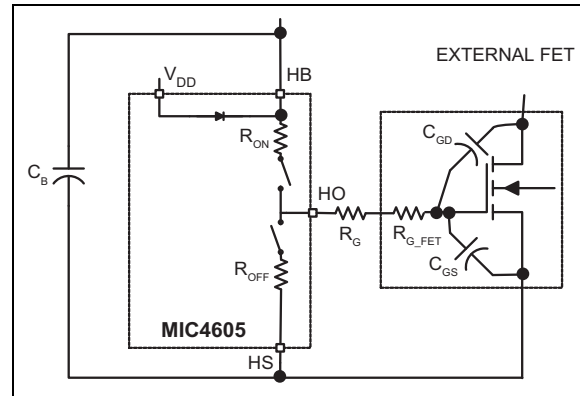
The MIC4605 [Typical Application Circuit](#) diagram illustrates how the MIC4605 drives the power stage of a DC motor. It is important that only one of the two MOSFETs is on at any given time. If both MOSFETs on the same side of the half-bridge are simultaneously on,  $V_{IN}$  will short to ground. The high current from the shorted  $V_{IN}$  supply will then “shoot through” the MOSFETs into ground. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing in the circuit. The high current and voltage ringing generate conducted and radiated EMI. [Table 7-1](#) illustrates truth tables for both the MIC4605-1 (dual TTL inputs) and MIC4605-2 (single PWM input) that details the “first on” priority as well as the failsafe delay.

**TABLE 7-1: MIC4605-1/-2 TRUTH TABLES**

LI	HI	LO	HO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	HO will not go high until LO falls below 1.9V.
1	0	1	0	LO will be delayed an extra 240 ns if HS never falls below 2.2V.
1	1	x	x	First on stays on until input of same goes low.
—	PWM	LO	HO	Comments
—	0	1	0	LO will be delayed an extra 240 ns if HS never falls below 2.2V.
—	1	0	1	HO will not go high until LO falls below 1.9V.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

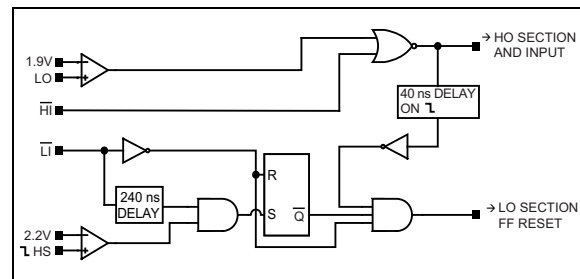
Adaptive dead time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on, even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. [Figure 7-1](#) shows an equivalent circuit of the gate driver section, including parasitics.



**FIGURE 7-1:** MIC4605 Driving an External MOSFET.

The internal gate resistance ( $R_{G\_FET}$ ) and any external damping resistor ( $R_G$ ) isolate the MOSFET’s gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used.

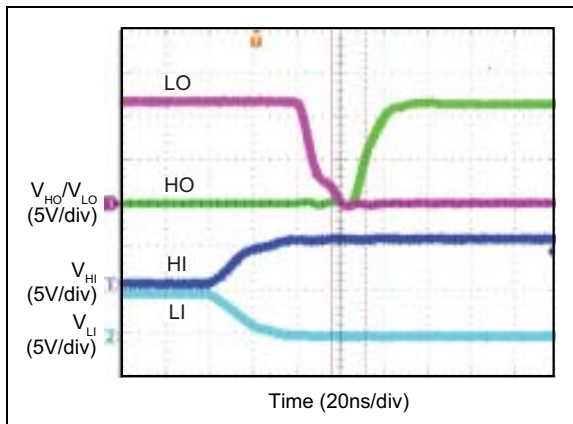
The MIC4605 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time, minimizing shoot-through current. [Figure 7-2](#) illustrates how the adaptive dead-time circuitry works.



**FIGURE 7-2:** Adaptive Dead-Time Logic Diagram (PWM).



Figure 7-3 shows the dead time (< 20 ns) between the gate drive output transitions as the low-side driver transitions from on to off, while the high-side driver transitions from off to on.



**FIGURE 7-3:** Adaptive Dead-Time LO (Low) to HO (High).

A high level on the PWM pin causes the LO pin to go low. The MIC4605 monitors the LO pin voltage and prevents the HO pin from turning on until the voltage on the LO pin reaches the  $V_{LOOFF}$  threshold. After a short delay, the MIC4605 drives the HO pin high. Monitoring the LO voltage eliminates any excessive delay due to the MOSFET drivers turn-off time, and the short delay accounts for the MOSFET turn-off delay, as well as letting the LO pin voltage settle out. An external resistor between the LO pin output and the MOSFET may affect the performance of the LO pin monitoring circuit and is not recommended.

A low on the PWM pin causes the HO pin to go low after a short delay ( $t_{HOFF}$ ). Before the LO pin can go high, the voltage on the switching node (HS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the HO pin voltage eliminates timing variations and excessive delays due to the high-side MOSFET turn-off. The LO driver turns on after a short delay ( $t_{LOON}$ ). Once the LO driver is turned on, it is latched on until the PWM signal goes high. This prevents any ringing or oscillations on the switch node, or the HS pin from turning off the LO driver. If the PWM pin goes low and the voltage on the HS pin does not cross the  $V_{SWTH}$  threshold, the LO pin will be forced high after a short delay ( $t_{SWTO}$ ), ensuring proper operation.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase-shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is determined by the time required for the  $C_B$  capacitor to charge during the off-time. Adequate time must be allowed for the  $C_B$  capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead-time circuit in the MIC4605 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti-shoot-through circuit's control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

## 7.2 HS Pin Clamp

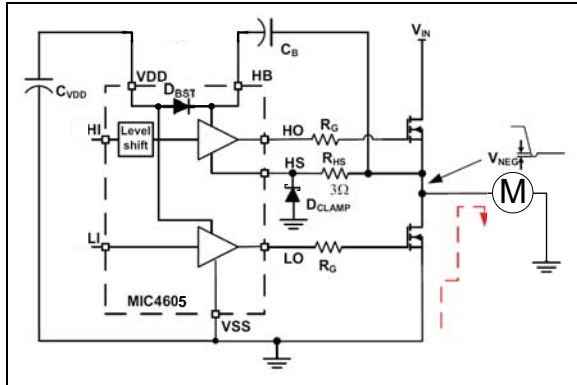
A resistor/diode clamp between the switch node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin.

Figure 7-4 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three-phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the On-Time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and possibly a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the HS pin voltage exceeds 0.7V, a diode or a Schottky diode between the HS pin and ground is recommended. The diode reverse voltage rating must be greater than the high-voltage input supply ( $V_{IN}$ ). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

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**FIGURE 7-4:** Negative HS Pin Voltage.

## 7.3 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

## 7.4 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the  $C_B$  capacitor, multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

### EQUATION 7-1:

$$I_{F(AVE)} = Q_{GATE} \times f_S$$

Where:

- $Q_{GATE}$  = Total Gate Charge at  $V_{HB} - V_{HS}$
- $f_S$  = Gate Drive Switching Frequency

The average power dissipated by the forward voltage drop of the diode equals:

### EQUATION 7-2:

$$P_{DIODEfwd} = I_{F(AVE)} \times V_F$$

Where:

- $V_F$  = Diode Forward Voltage Drop

The value of  $V_F$  should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of  $V_F$  at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically  $3 \mu A$  at a reverse voltage of  $85V$  at  $+125^\circ C$ . Power dissipation due to reverse leakage is typically much less than  $1 mW$  and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated by computing the average reverse current due to reverse recovery charge times the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by:

### EQUATION 7-3:

$$I_{RR(AVE)} = 0.5 \times I_{RRM} \times t_{RR} \times f_S$$

Where:

- $I_{RRM}$  = Peak Reverse Recovery Current
- $t_{RR}$  = Reverse Recovery Time

### EQUATION 7-4:

$$P_{DIODErr} = I_{RR(AVE)} \times V_{REV}$$

The total diode power dissipation is:

### EQUATION 7-5:

$$P_{DIODEtotal} = P_{DIODEfwd} + P_{DIODErr}$$

An optional external bootstrap diode may be used instead of the internal diode (Figure 7-5). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the  $V_{DD}$  supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

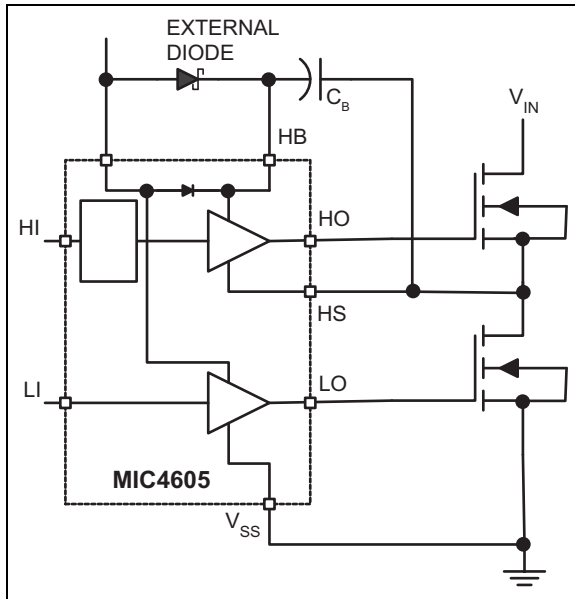
### EQUATION 7-6:

$$P_{DIODErev} = I_R \times V_{REV} \times (1 - D)$$

Where:

- $I_R$  = Reverse Current Flow at  $V_{REV}$  and  $T_J$
- $V_{REV}$  = Diode Reverse Voltage
- $D$  = Duty Cycle ( $t_{ON} \times f_S$ )

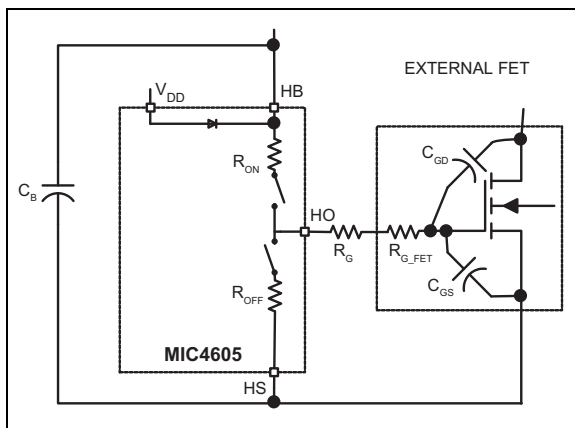
The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.



**FIGURE 7-5:** Optional Bootstrap Diode.

## 7.5 Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 7-6 shows a simplified equivalent circuit of the MIC4605 driving an external MOSFET.



**FIGURE 7-6:** MIC4605 Driving an External MOSFET.

### 7.5.1 DISSIPATION DURING THE EXTERNAL MOSFET TURN-ON

Energy from capacitor  $C_B$  is used to charge up the input capacitance of the MOSFET ( $C_{GD}$  and  $C_{GS}$ ). The energy delivered to the MOSFET is dissipated in the three resistive components,  $R_{ON}$ ,  $R_G$  and  $R_{G\_FET}$ .  $R_{ON}$  is the on-resistance of the upper driver MOSFET in the MIC4605.  $R_G$  is the series resistor (if any) between the driver IC and the MOSFET.  $R_{G\_FET}$  is the gate resistance of the MOSFET.  $R_{G\_FET}$  is usually listed in the power MOSFET's specifications. The ESR of capacitor  $C_B$  and the resistance of the connecting etch can be ignored because they are much less than  $R_{ON}$  and  $R_{G\_FET}$ .

The effective capacitances of  $C_{GD}$  and  $C_{GS}$  are difficult to calculate because they vary nonlinearly with  $I_D$ ,  $V_{GS}$  and  $V_{DS}$ . Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus  $V_{GS}$ . Figure 7-7 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5 nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

#### EQUATION 7-7:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^2$$

but

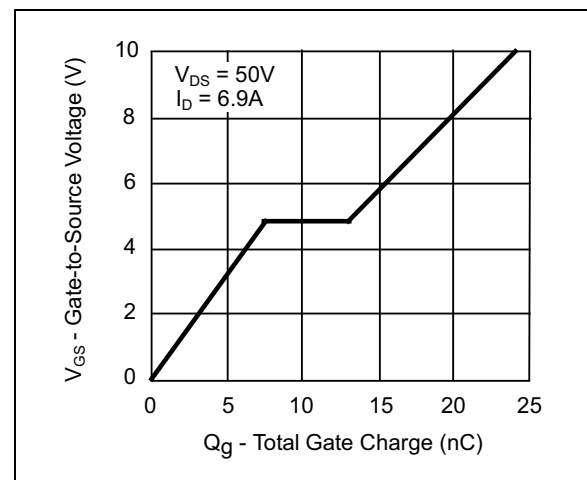
$$Q = C \times V$$

so

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where:

$C_{ISS}$  = Total Gate Capacitance of the MOSFET



**FIGURE 7-7:** Typical Gate Charge vs.  $V_{GS}$ .

# MIC4605

The same energy is dissipated by  $R_{OFF}$ ,  $R_G$  and  $R_{G\_FET}$  when the driver IC turns the MOSFET off. Assuming  $R_{ON}$  is approximately equal to  $R_{OFF}$ , the total energy and power dissipated by the resistive drive elements is:

## EQUATION 7-8:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

$E_{DRIVER}$  = Energy Dissipated per Switching Cycle

$P_{DRIVER}$  = Power Dissipated per Switching Cycle

$Q_G$  = Total Gate Charge at  $V_{GS}$

$V_{GS}$  = Gate-to-Source Voltage on the MOSFET

$f_S$  = Switching Frequency of the Gate Drive Circuit

The power dissipated inside the MIC4605 is equal to the ratio of  $R_{ON}$  and  $R_{OFF}$  to the external resistive losses in  $R_G$  and  $R_{G\_FET}$ . Letting  $R_{ON} = R_{OFF}$ , the power dissipated in the MIC4605 due to driving the external MOSFET is:

## EQUATION 7-9:

$$P_{DISSdriver} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$

## 7.6 Supply Current Power Dissipation

Power is dissipated in the MIC4605 even if nothing is being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry and the shoot-through current in the output drivers. The supply current is proportional to the operating frequency and the  $V_{DD}$  and  $V_{HB}$  voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4605 due to supply current is:

## EQUATION 7-10:

$$P_{DISSsupply} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB}$$

## 7.7 Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4605 is equal to the power dissipation caused by driving the external MOSFETs, the supply current and the internal bootstrap diode.

## EQUATION 7-11:

$$P_{DISStotal} = P_{DISSsupply} + P_{DISSdrive} + P_{DIODEtotal}$$

The die temperature can be calculated after the total power dissipation is known.

## EQUATION 7-12:

$$T_J = T_A + P_{DISStotal} \times \theta_{JA}$$

Where:

$T_J$  = Junction Temperature ( $^{\circ}\text{C}$ )

$T_A$  = Maximum Ambient Temperature

$P_{DISStotal}$  = Power Dissipation of the MIC4605

$\theta_{JA}$  = Thermal Resistance from Junction to Ambient Air

## 7.8 Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the  $C_B$  capacitor to charge during the off-time. Adequate time must be allowed for the  $C_B$  capacitor to charge up before the high-side driver is turned on.

## 7.9 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side ( $V_{DD}$ ) and high-side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from HB to HS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U-type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1  $\mu\text{F}$  is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low-voltage capacitors are used, because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for  $V_{DD}$  should be placed as close as possible between the  $V_{DD}$  and  $V_{SS}$  pins. The bypass capacitor ( $C_B$ ) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to [Section 7.12 “Grounding, Component Placement and Circuit Layout”](#) for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus  $V_{GS}$  voltage. Based on this information and a recommended  $\Delta V_{HB}$  of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

### EQUATION 7-13:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}}$$

Where:

$$Q_{GATE} = \text{Total Gate Charge at } V_{HB}$$

$$\Delta V_{HB} = \text{Voltage Drop at the HB Pin}$$

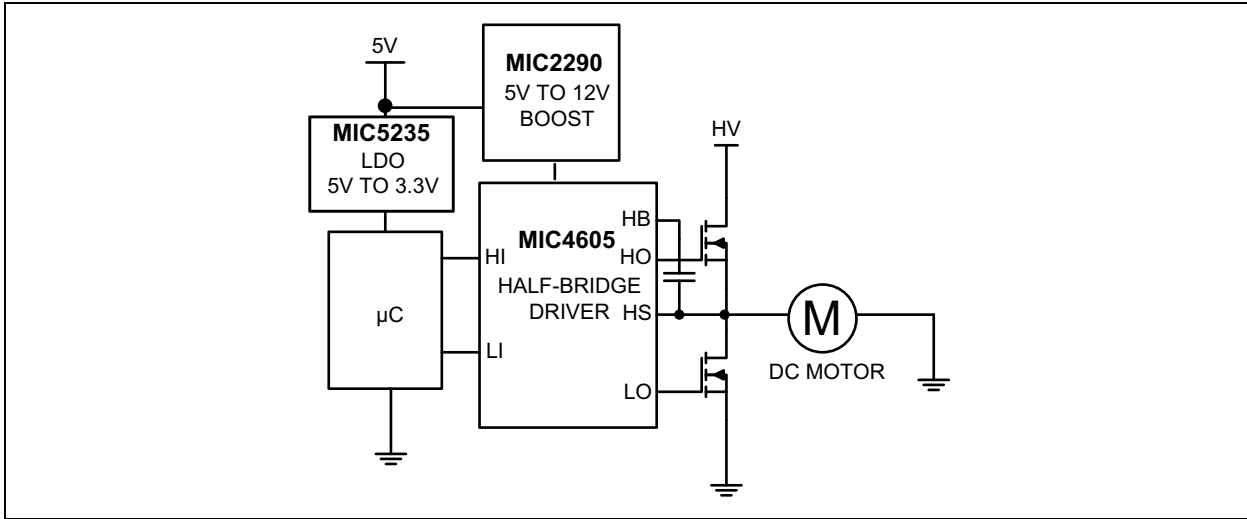
The decoupling capacitor for the  $V_{DD}$  input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

## 7.10 DC Motor Applications

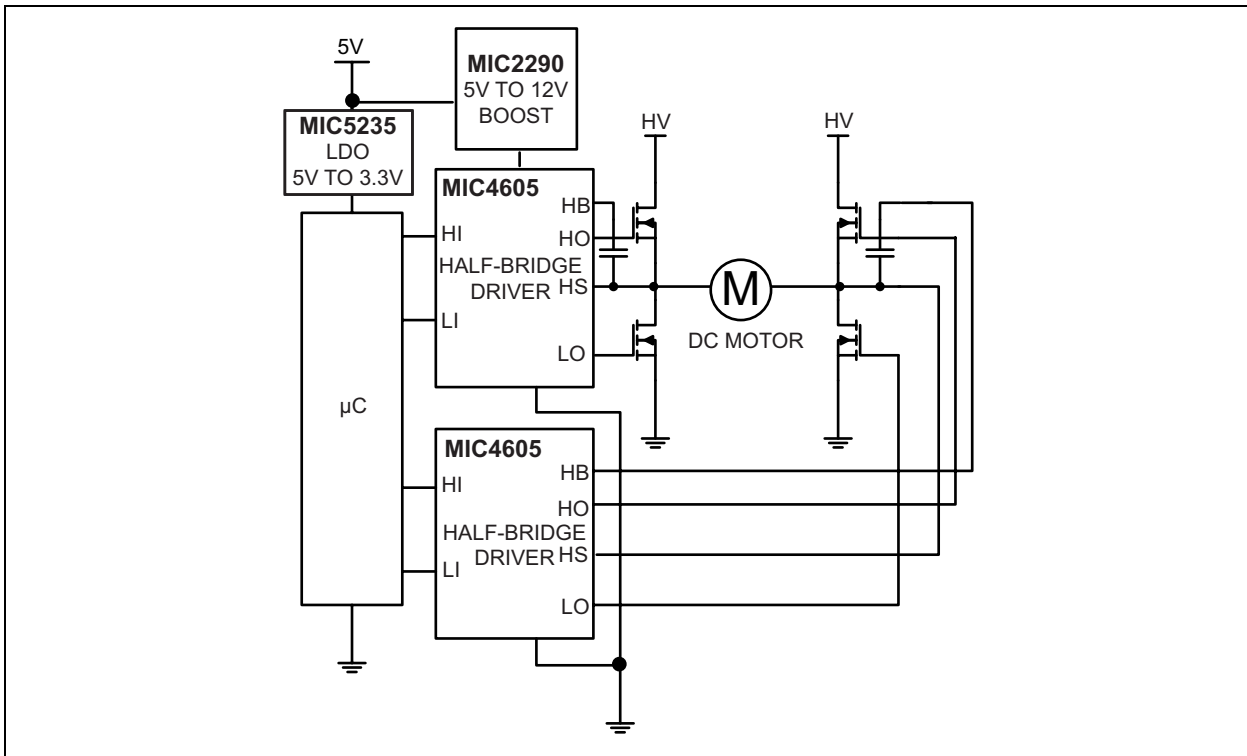
MIC4605 MOSFET drivers are widely used in DC motor applications. They address brushed motors in both half-bridge and full-bridge motor topologies, as well as 3-phase brushless motors. As shown in [Figure 7-8](#), [Figure 7-9](#) and [Figure 7-10](#), the drivers switch the MOSFETs at variable duty cycles that modulate the voltage to control motor speed. In the half-bridge topology, the motor turns in one direction only. The full-bridge topology allows for bidirectional control. Three-phase motors are more efficient as compared to the brushed motors, but require three half-bridge switches and additional circuitry to sense the position of the rotor.

The MIC4605 85V operating voltage offers the engineer a margin to protect against Back Electromotive Force (EMF), which is a voltage spike caused by the rotation of the rotor. The Back EMF voltage amplitude depends on the speed of the rotation. It is good practice to have at least twice the HV voltage of the motor supply; 85V is plenty of margin for 12V, 24V and 40V motors.

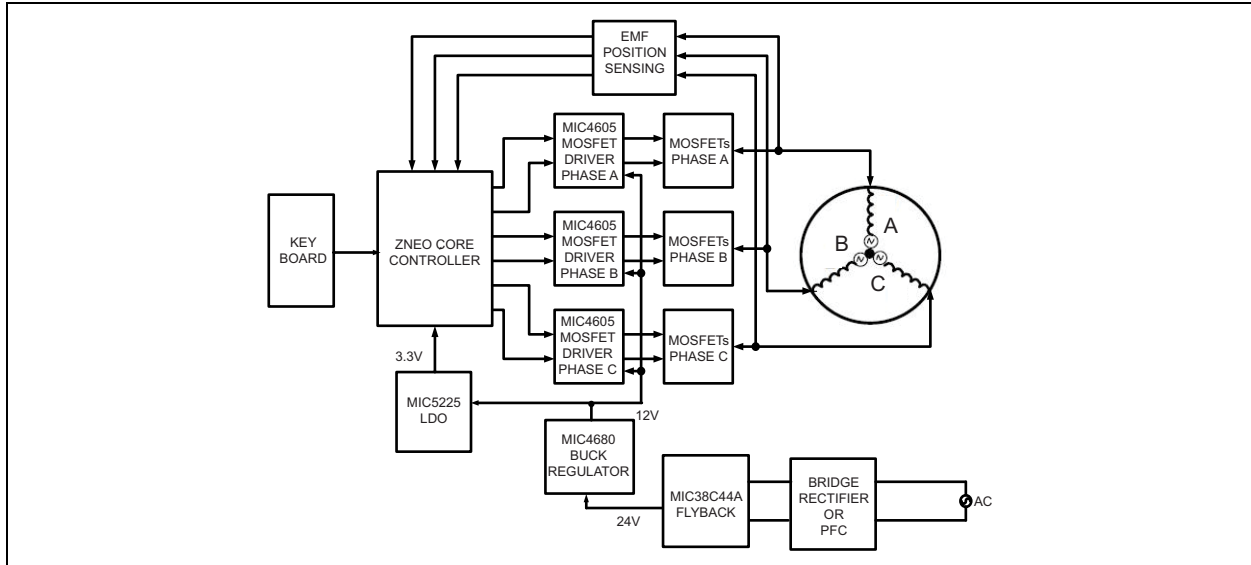
# MIC4605



**FIGURE 7-8:** Half-Bridge DC Motor.



**FIGURE 7-9:** Full-Bridge DC Motor.



**FIGURE 7-10:** 3-Phase Brushless DC Motor Driver – 24V Block Diagram.

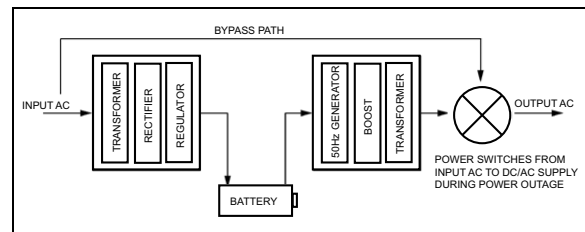
The MIC4605 is offered in a small 2.5 mm x 2.5 mm TDFN package for applications that are space constrained and an 8-lead SOIC package for ease of manufacturing. The motor trend is to put the motor control circuit inside the motor casing, which requires small packaging because of the size of the motor.

The MIC4605 offers low UVLO threshold and programmable gate drive, which allows for longer operation time in battery-operated motors, such as power hand tools.

Cross conduction across the half bridge can cause catastrophic failure in a motor application. Engineers typically add dead time between states that switch between high input and low input to ensure that the low-side MOSFET completely turns off before the high-side MOSFET turns on and vice versa. The dead time depends on the MOSFET used in the application, but 200 ns is typical for most motor applications.

## 7.11 Power Inverter

Power inverters are used to supply AC loads from a DC operated battery system, mainly during power failure. The battery voltage can be 12 VDC, 24 VDC or up to 36 VDC, depending on the power requirements. There are two popular conversion methods: Type I and Type II that convert the battery energy to AC line voltage (110 VAC or 230 VAC).



**FIGURE 7-11:** Type I Inverter Topology.

As shown in Figure 7-11, Type I is a dual stage topology, where line voltage is converted to DC through a transformer to charge the storage batteries. When a power failure is detected, the stored DC energy is converted to AC through another transformer to drive the AC loads connected to the inverter output. This method is simplest to design, but tends to be bulky and expensive because it uses two transformers.

Type II is a single-stage topology that uses only one transformer to charge the bank of batteries to store the energy. During a power outage, the same transformer is used to power the line voltage. The Type II switches at a higher frequency as compared to the Type I topology to maintain a small transformer size.

Both types require a half-bridge or full-bridge topology to boost the DC to AC. This application can use two MIC4605s. The 85V operating voltage offers enough margin to address all of the available banks of batteries commonly used in inverter applications. The 85V operating voltage allows designers to increase the bank of batteries up to 72V, if desired. The MIC4605 can sink as much as 1A, which is enough current to overcome the MOSFET's input capacitance and switch the MOSFET up to 50 kHz. This makes the MIC4605 an ideal solution for inverter applications.



# MIC4605

As with all half-bridge and full-bridge topologies, cross conduction is a concern to inverter manufacturers because it can cause catastrophic failure. This can be remedied by adding the appropriate dead time between transitioning from the high-side MOSFET to the low-side MOSFET and vice versa.

## 7.12 Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4605 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing or circuit latch-up.

Figure 7-12 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low-impedance ground plane. Charge needed to turn on the MOSFET gates comes from the decoupling capacitors,  $C_{VDD}$  and  $C_B$ . Current in the low-side gate driver flows from  $C_{VDD}$  through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor  $C_B$  and flows into the HB pin and out the HO pin, into the gate of the high-side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor  $C_B$ . The high-side circuit return path usually does not have a low-impedance ground plane, so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor  $C_B$  must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on, but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

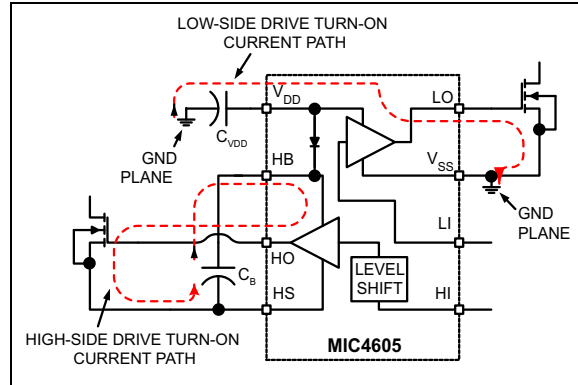


FIGURE 7-12: Turn-On Current Paths.

Figure 7-13 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor,  $C_B$ .

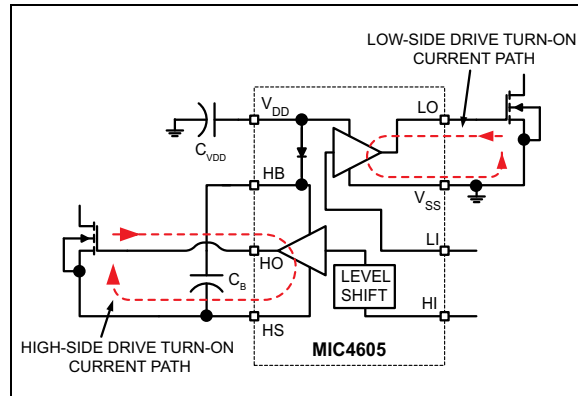


FIGURE 7-13: Turn-Off Current Paths.





# MIC4605

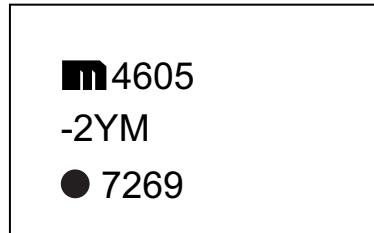
## 8.0 PACKAGING INFORMATION

### 8.1 Package Marking Information

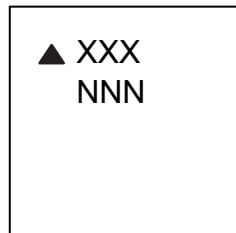
8-Pin SOIC\*



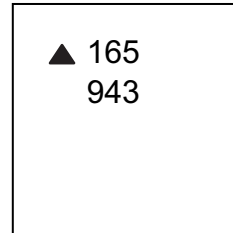
Example



10-Pin TDFN\*



Example



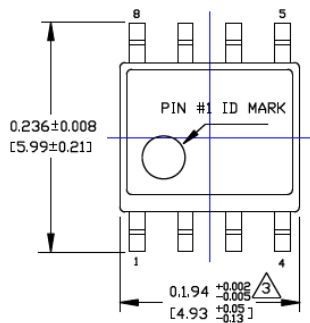
<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (¯) symbol may not be to scale.	

## 8-Lead SOIC Package Outline and Recommended Land Pattern

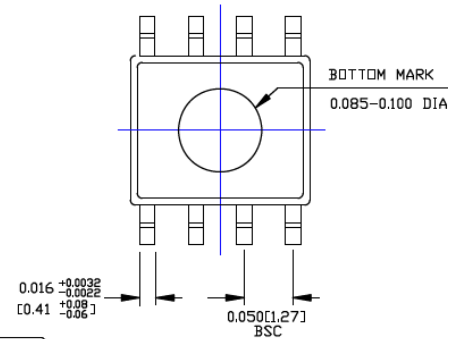
**TITLE**

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

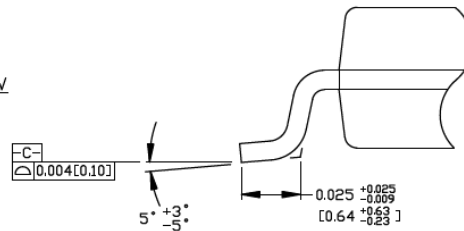
DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]
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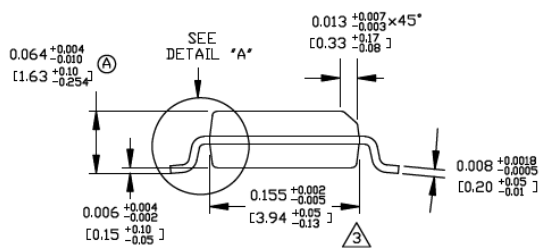
TOP VIEW



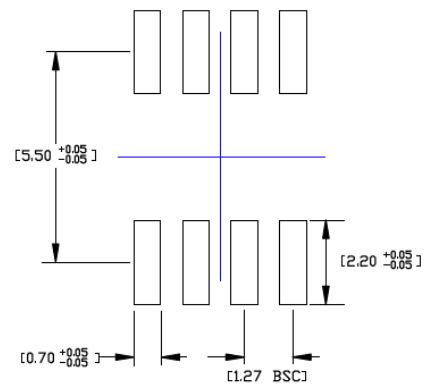
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

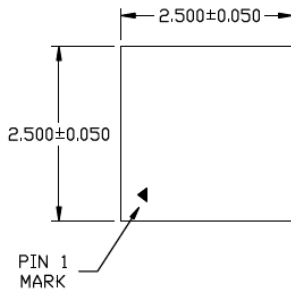
# MIC4605

## 10-Lead TDFN 2.5 mm x 2.5 mm Package Outline and Recommended Land Pattern

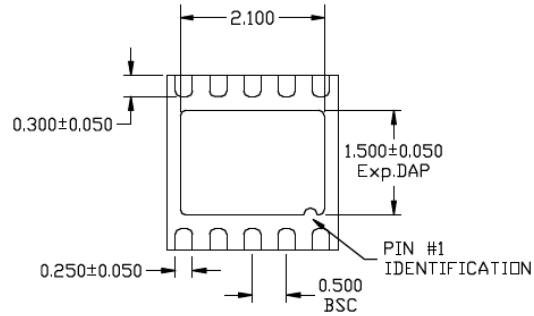
**TITLE**

10 LEAD TDFN 2.5x2.5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

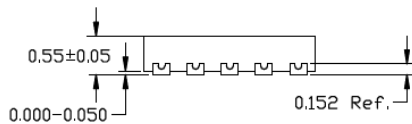
DRAWING #	TDFN2525-10LD-PL-1	UNIT	MM
Lead Frame	Copper	Lead Finish	Matte Tin



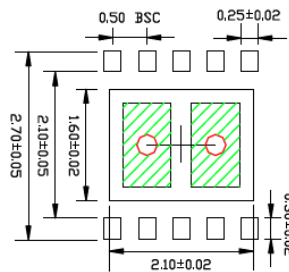
**TOP VIEW**  
NOTE: 1, 2, 3



**BOTTOM VIEW**  
NOTE: 1, 2



**SIDE VIEW**  
NOTE: 1, 2



**RECOMMENDED LAND PATTERN**  
NOTE: 4

**NOTE:**

1. MAX PACKAGE WARPAGE IS 0.05MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN RECTANGLES (SHADED AREA) INDICATE STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.6X0.9MM, SPACING IS 0.3MM.
5. RED CIRCLES REPRESENT THERMAL VIAS & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30 - 0.35 MM RECOMMENDED DIAMETER, 1.00 MM PITCH

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision E (December 2019)

- Updated [Typical Application Circuit](#).
- Updated [Section 7.2 “HS Pin Clamp”](#).
- Updated [Figure 7-4](#).

### Revision D (August 2019)

- Updated [Section 6.2, Enable Input](#).

### Revision C (June 2019)

- Updated [Section 1.0, Electrical Characteristics](#).

### Revision B (August 2018)

- AEC-Q100 qualification.

### Revision A (January 2018)

- Converted Micrel document MIC4605 to Microchip data sheet DS20005853A.
- Minor text changes throughout.
- Added [Section 7.2 “HS Pin Clamp”](#).

# MIC4605

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NOTES:

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To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		<u>-X</u>	<u>X</u>	<u>XX</u>	<u>-XX</u>
Device	Input Option	Temperature	Package	Media Type	
<b>Device:</b>	MIC4605:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection			
<b>Input Option:</b>	-1	=	Dual inputs		
	-2	=	Single PWM input		
<b>Temperature:</b>	Y	=	-40°C to +125°C		
<b>Package:</b>	M	=	8-Lead SOIC		
	MT	=	10-Lead 2.5 mm x 2.5 mm TDFN		
<b>Media Type:</b>	<blank>	=	95/Tube		
	T5	=	500/Reel		
	TR	=	2,500/Reel		

<b>Examples:</b>	
a) MIC4605-1YM:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection, Dual Inputs, -40°C to +125°C, 8-Lead SOIC, 95/Tube
b) MIC4605-2YM-T5:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection, Single PWM Input, -40°C to +125°C, 8-Lead SOIC, 500/Reel
c) MIC4605-1YM-TR:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection, Dual Inputs, -40°C to +125°C, 8-Lead SOIC, 2,500/Reel
d) MIC4605-2YMT:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection, Single PWM Input, -40°C to +125°C, 10-Lead TDFN, 95/Tube
e) MIC4605-1YMT-T5:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection, Dual Inputs, -40°C to +125°C, 10-Lead TDFN, 500/Reel
f) MIC4605-2YMT-TR:	85V Half-Bridge MOSFET Driver with Adaptive Dead Time and Shoot-Through Protection, Single PWM Input, -40°C to +125°C, 10-Lead TDFN, 2,500/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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NOTES:



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