

FEATURES

- Complies with ANSI TIA/EIA-485-A-1998 and ISO 8482: 1987(E)
- 250 kbps data rate
- ±4 kV HBM ESD protection on all pins
- Single 5 V ± 10% supply
- 7 V to +12 V bus common-mode range
- Connect up to 32 nodes on the bus
- Reduced slew rate for low EM interference
- Short-circuit protection
- 30 µA supply current

APPLICATIONS

- Low power RS-485 and RS-422 systems
- DTE-DCE interface
- Packet switching
- Local area networks
- Data concentration
- Data multiplexers
- Integrated services digital network (ISDN)

GENERAL DESCRIPTION

The [ADM488A](#) and [ADM489A](#) are low power, differential line transceivers suitable for communication on multipoint bus transmission lines. They are intended for balanced data transmission and comply with both RS-485 and RS-422 standards of the Electronics Industries Association (EIA). Both products contain a single differential line driver and a single differential line receiver, making them suitable for full-duplex data transfer. The [ADM489A](#) contains an additional receiver and driver enable control.

The input impedance is 12 kΩ, allowing 32 transceivers to be connected on the bus. The [ADM488A/ADM489A](#) operate from a single 5 V ± 10% power supply.

FUNCTIONAL BLOCK DIAGRAMS

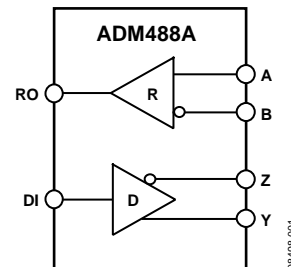


Figure 1. [ADM488A](#)

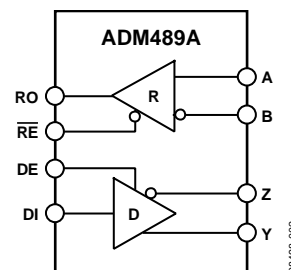


Figure 2. [ADM489A](#)

Excessive power dissipation that is caused by bus contention or output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The [ADM488A/ADM489A](#) are fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology.

The [ADM488A/ADM489A](#) are fully specified over the industrial temperature range and are available in SOIC and MSOP packages.

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REVISION HISTORY

6/14—Rev. A to Rev. B

| | |
|----------------------------------|---|
| Changes to Features Section..... | 1 |
| Changes to Table 3..... | 5 |

11/10—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Table 2..... | 4 |
| Changes to Figure 20..... | 11 |
| Changes to Figure 21..... | 12 |
| Added New Figure 23, Renumbered Subsequent Figures, Moved Old Figure 23 to New Figure 25 | 14 |
| Changes to Ordering Guide | 15 |

10/09—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 10\%$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------------|------|-----|-----------|---------------|---|
| DRIVER | | | | | | |
| Differential Output Voltage | V_{OD} | | | 5.0 | V | $R = \infty$, see Figure 11 |
| | | 2.0 | | 5.0 | V | $V_{CC} = 5\text{ V}$, $R = 50\ \Omega$ (RS-422), see Figure 11 |
| | | 1.5 | | 5.0 | V | $R = 27\ \Omega$ (RS-485), see Figure 11 |
| | | 1.5 | | 5.0 | V | $V_{TST} = -7\text{ V to } +12\text{ V}$, see Figure 12, $V_{CC} = 5\text{ V} \pm 5\%$ |
| $\Delta V_{OD} $ for Complementary Output States | | | | 0.2 | V | $R = 27\ \Omega$ or $50\ \Omega$, see Figure 11 |
| Common-Mode Output Voltage | V_{OC} | | | 3.0 | V | $R = 27\ \Omega$ or $50\ \Omega$, see Figure 11 |
| $\Delta V_{OC} $ for Complementary Output States | | | | 0.2 | V | $R = 27\ \Omega$ or $50\ \Omega$ |
| Output Short-Circuit Current | | | | 250 | mA | $-7\text{ V} \leq V_O \leq +12\text{ V}$ |
| V_{OUT} | | | | | | |
| CMOS Input Logic Threshold Low | V_{INL} | | 1.4 | 0.8 | V | |
| CMOS Input Logic Threshold High | V_{INH} | 2.0 | 1.4 | | V | |
| Logic Input Current (DE, DI) | | | | ± 1.0 | μA | |
| RECEIVER | | | | | | |
| Differential Input Threshold Voltage | V_{TH} | -0.2 | | +0.2 | V | $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$ |
| Input Voltage Hysteresis | ΔV_{TH} | | 70 | | mV | $V_{CM} = 0\text{ V}$ |
| Input Resistance | | 12 | | | k Ω | $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$ |
| Input Current (A, B) | | | | 1 | mA | $V_{IN} = 12\text{ V}$ |
| | | | | -0.8 | mA | $V_{IN} = -7\text{ V}$ |
| Logic Enable Input Current (\overline{RE}) | | | | ± 1 | μA | |
| CMOS Output Voltage Low | V_{OL} | | | 0.4 | V | $I_{OUT} = +4.0\text{ mA}$ |
| CMOS Output Voltage High | V_{OH} | 4.0 | | | V | $I_{OUT} = -4.0\text{ mA}$ |
| Short-Circuit Output Current | | 7 | | 85 | mA | $V_{OUT} = \text{GND or } V_{CC}$ |
| Three-State Output Leakage Current | | | | ± 1.0 | μA | $0.4\text{ V} \leq V_{OUT} \leq 2.4\text{ V}$ |
| POWER SUPPLY CURRENT | | | | | | |
| | I_{CC} | | 30 | 60 | μA | Outputs unloaded, receivers enabled |
| | | | 37 | 74 | μA | DE = 0 V (disabled) |
| | | | | | | DE = 5 V (enabled) |

TIMING SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 10\%$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------------------------|-----------------------|-----|-----|------|------|---|
| DRIVER | | | | | | |
| Propagation Delay Input to Output | t_{PLH}, t_{PHL} | 250 | | 2000 | ns | R_L differential = 54 Ω , $C_{L1} = C_{L2} = 100$ pF, see Figure 15, Figure 16 |
| Driver Output Skew | t_{SKEW} | | 100 | 800 | ns | R_L differential = 54 Ω , $C_{L1} = C_{L2} = 100$ pF, see Figure 15 |
| Driver Rise/Fall Time | t_{DR}, t_{DF} | 250 | | 2000 | ns | R_L differential = 54 Ω , $C_{L1} = C_{L2} = 100$ pF, see Figure 15, Figure 16 |
| Driver Enable to Output Valid | t_{ZL}, t_{ZH} | 250 | | 2000 | ns | $R_L = 500$ Ω , $C_L = 100$ pF, see Figure 12, Figure 18 |
| Driver Disable Timing | t_{LZ}, t_{HZ} | 300 | | 3000 | ns | $R_L = 500$ Ω , $C_L = 15$ pF, see Figure 12, Figure 18 |
| Maximum Data Rate | | 250 | | | kbps | |
| RECEIVER | | | | | | |
| Propagation Delay Input to Output | t_{PLH}, t_{PHL} | 250 | | 2000 | ns | $C_L = 15$ pF, see Figure 15, Figure 17 |
| Skew | $ t_{PLH} - t_{PHL} $ | | 100 | | ns | |
| Receiver Enable | t_{EN1} | | 10 | 50 | ns | $R_L = 1$ k Ω , $C_L = 15$ pF, see Figure 14, Figure 19 |
| Receiver Disable | t_{EN2} | | 10 | 50 | ns | $R_L = 1$ k Ω , $C_L = 15$ pF, see Figure 14, Figure 19 |
| Maximum Data Rate | | 250 | | | kbps | |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|--|---|
| V_{CC} | 7 V |
| Inputs | |
| Driver Input (DI) | $-0.3\text{ V to }V_{CC} + 0.3\text{ V}$ |
| Control Inputs (DE, $\overline{\text{RE}}$) | $-0.3\text{ V to }V_{CC} + 0.3\text{ V}$ |
| Receiver Inputs (A, B) | $-14\text{ V to }+14\text{ V}$ |
| Outputs | |
| Driver Outputs | $-14\text{ V to }+12.5\text{ V}$ |
| Receiver Output | $-0.5\text{ V to }V_{CC} + 0.5\text{ V}$ |
| Power Dissipation 8-Lead SOIC | 520 mW |
| θ_{JA} , Thermal Impedance | 110°C/W |
| Power Dissipation 14-Lead SOIC | 800 mW |
| θ_{JA} , Thermal Impedance | 120°C/W |
| Operating Temperature Range | |
| Industrial (A Version) | $-40^\circ\text{C to }+85^\circ\text{C}$ |
| Storage Temperature Range | $-65^\circ\text{C to }+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD Protection on All Pins | |
| Human Body Model (HBM) | $\pm 4\text{ kV}$ |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

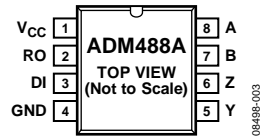


Figure 3. ADM488A SOIC_N and MSOP Pin Configuration

Table 4. ADM488A Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|--|
| 1 | V _{CC} | Power Supply, 5 V ± 10%. |
| 2 | RO | Receiver Output. When A > B by 200 mV, RO = high. If A < B by 200 mV, RO = low. |
| 3 | DI | Driver Input. A logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low. |
| 4 | GND | Ground Connection, 0 V. |
| 5 | Y | Noninverting Driver, Differential Output Y. |
| 6 | Z | Inverting Driver, Differential Output Z. |
| 7 | B | Inverting Receiver, Input B. |
| 8 | A | Noninverting Receiver, Input A. |



Figure 4. ADM489A SOIC_N Pin Configuration



Figure 5. ADM489A MSOP Pin Configuration

Table 5. ADM489A Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|----------|------------------|-----------------|---|
| SOIC_N | MSOP | | |
| 1, 8, 13 | N/A ¹ | NC | No Connect. No connections are required to this pin. |
| 2 | 1 | RO | Receiver Output. When enabled, if A > B by 200 mV, RO = high. If A < B by 200 mV, RO = low. |
| 3 | 2 | RE | Receiver Output Enable. A low level enables the receiver output, RO. A high level places the ADM489A in a high impedance state. |
| 4 | 3 | DE | Driver Output Enable. A high level enables the driver differential outputs (Y and Z). A low level places the ADM489A in a high impedance state. |
| 5 | 4 | DI | Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low. |
| 6, 7 | 5 | GND | Ground Connection, 0 V. |
| 9 | 6 | Y | Noninverting Driver, Differential Output Y. |
| 10 | 7 | Z | Inverting Driver, Differential Output Z. |
| 11 | 8 | B | Inverting Receiver, Input B. |
| 12 | 9 | A | Noninverting Receiver, Input A. |
| 14 | 10 | V _{CC} | Power Supply, 5 V ± 10%. |

¹ N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

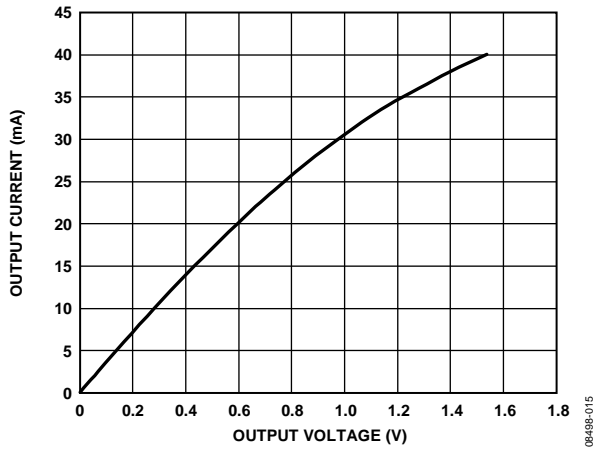


Figure 6. Output Current vs. Receiver Output Low Voltage

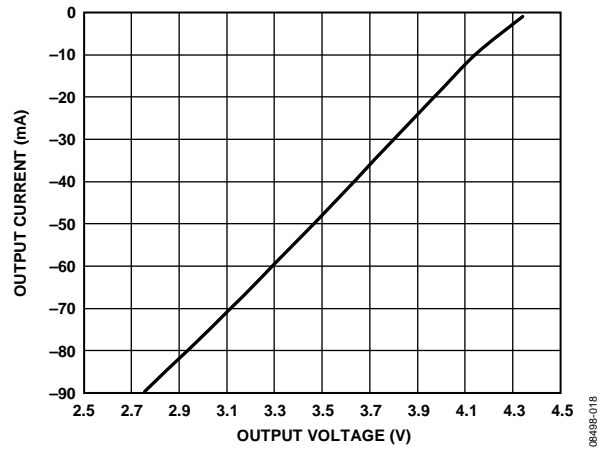


Figure 9. Output Current vs. Driver Output High Voltage

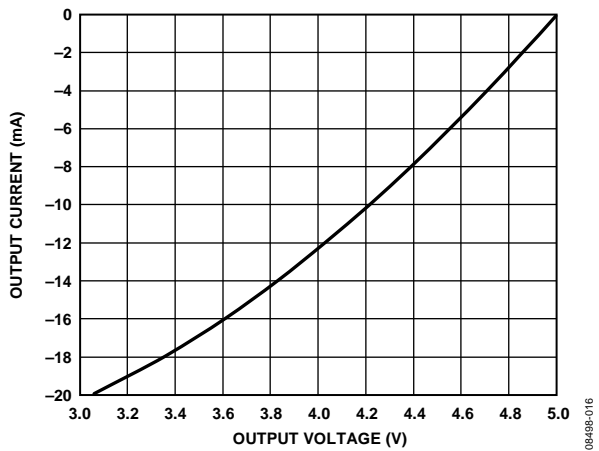


Figure 7. Output Current vs. Receiver Output High Voltage

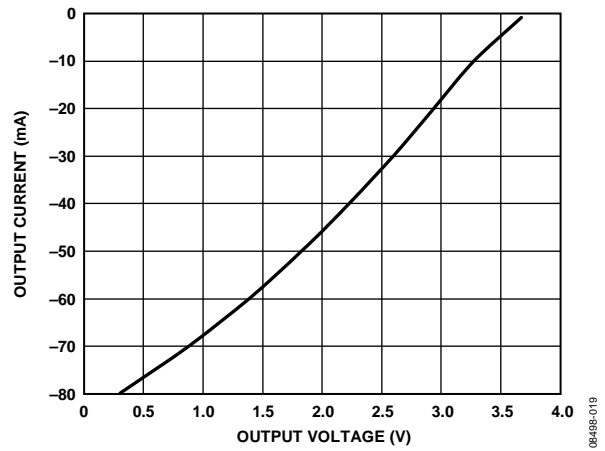


Figure 10. Output Current vs. Driver Differential Output Voltage



Figure 8. Output Current vs. Driver Output Low Voltage

TEST CIRCUITS

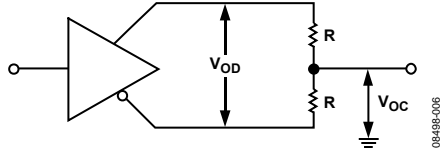


Figure 11. Driver Voltage Measurement Test Circuit



Figure 14. Receiver Enable/Disable Test Circuit

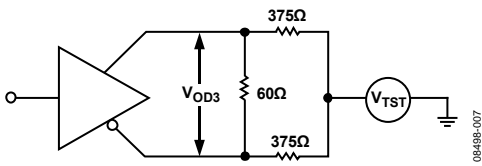


Figure 12. Driver Enable/Disable Test Circuit

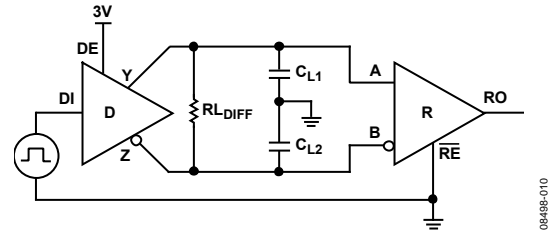


Figure 15. Driver/Receiver Propagation Delay Test Circuit



Figure 13. Driver Voltage Measurement Test Circuit

SWITCHING CHARACTERISTICS

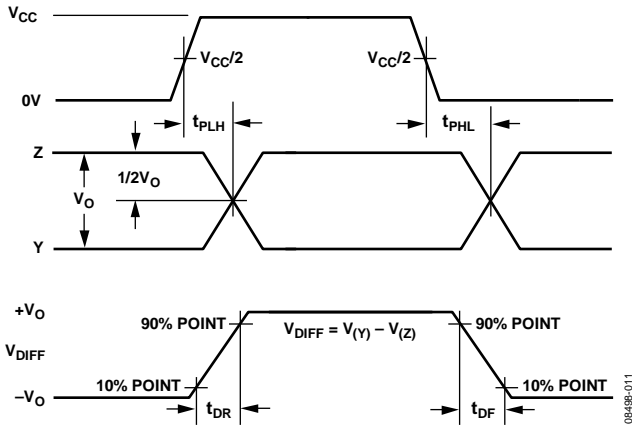


Figure 16. Driver Propagation Delay, Rise/Fall Timing

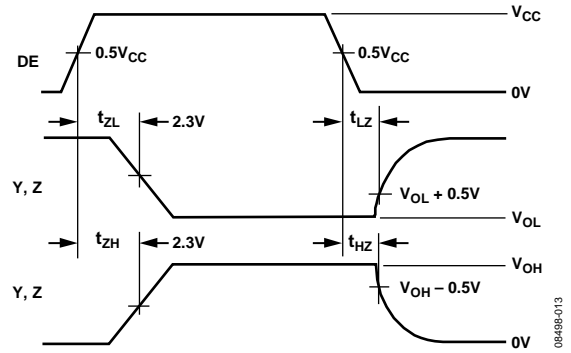


Figure 18. Driver Enable/Disable Timing

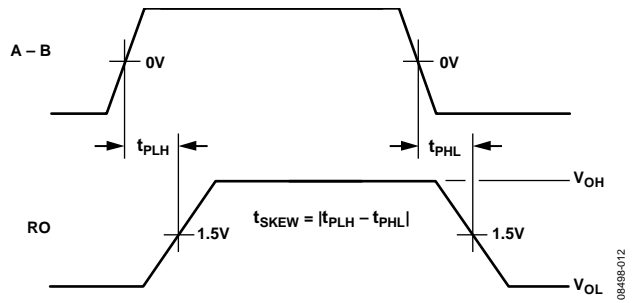


Figure 17. Receiver Propagation Delay

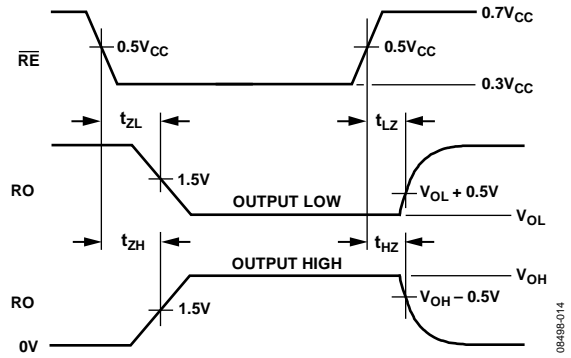


Figure 19. Receiver Enable/Disable Timing

THEORY OF OPERATION

The ADM488A/ADM489A are ruggedized RS-485 transceivers that operate from a single 5 V supply. They contain protection against radiated and conducted interference and are ideally suited for operation in electrically harsh environments or where cables can be plugged/unplugged. They are also immune to high RF field strengths without special shielding precautions.

The ADM488A/ADM489A are intended for balanced data transmission and comply with both EIA RS-485 and RS-422 standards. They contain a differential line driver and a differential line receiver, and are suitable for full-duplex data transmission.

The input impedance on the ADM488A/ADM489A is 12 kΩ, allowing up to 32 transceivers on the differential bus. The ADM488A/ADM489A operate from a single 5 V ± 10% power supply. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM488A/ADM489A can transmit at data rates up to 250 kbps. Figure 20 shows a typical application for the ADM488A/ADM489A, a full-duplex link where data transfers at rates of up to 250 kbps. A terminating resistor is shown at both ends of the link. This termination is not critical because

the slew rate is controlled by the ADM488A/ADM489A and reflections are minimized.

The communications network can be extended to include multipoint connections, as shown in Figure 22. As many as 32 transceivers can be connected to the bus.

Table 6 and Table 7 show the truth tables for transmitting and receiving.

Table 6. Transmitting Truth Table

| Inputs | | | Outputs | |
|----------------|----|----------------|---------|--------|
| RE | DE | DI | Z | Y |
| X ¹ | 1 | 1 | 0 | 1 |
| X ¹ | 1 | 0 | 1 | 0 |
| 0 | 0 | X ¹ | High-Z | High-Z |
| 1 | 0 | X ¹ | High-Z | High-Z |

¹ X is don't care.

Table 7. Receiving Truth Table

| Inputs | | | Output |
|--------|----|---------------------|--------|
| RE | DE | A to B | RO |
| 0 | 0 | ≥ +0.2 V | 1 |
| 0 | 0 | ≤ -0.2 V | 0 |
| 0 | 0 | Inputs open circuit | 1 |
| 1 | 0 | X ¹ | High-Z |

¹ X is don't care.



NOTES
1. MAXIMUM NUMBER OF NODES = 32.

Figure 20. ADM488A/ADM489A Full-Duplex Data Link

084488-021

MAXIMUM NUMBER OF NODES = 32



NOTES
 1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 21. Typical RS-485 Full-Duplex Application

08488-023

APPLICATIONS INFORMATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission reliably transmits data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals, which appear as common-mode voltages on the line. Two main standards that specify the electrical characteristics of transceivers used in differential data transmission are approved by the EIA.

The RS-422 standard specifies data rates up to 10 Mbps and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

To cater to true multipoint communications, the RS-485 standard was defined to meet or exceed the requirements of RS-422. It also allows up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of -7 V to $+12\text{ V}$ is defined. The most significant difference between the RS-422 and RS-485 is that the RS-485 drivers can be disabled, thereby allowing up to 32 receivers to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM488A/ADM489A are designed for bidirectional data communications on multipoint transmission lines. A typical application with a multipoint transmission network is illustrated in Figure 22. An RS-485 transmission line can have up to 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers can be simultaneously enabled.

As with any transmission line, it is important to minimize reflections. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Keep stub lengths of the main line as short as possible. A properly terminated transmission line appears purely resistive to the driver.

Table 8. Comparison of RS-422 and RS-485 Interface Standards

| Specification | RS-422 | RS-485 |
|--------------------------------------|--------------------------------|---------------------------------|
| Transmission Type | Differential | Differential |
| Maximum Data Rate | 10 Mbps | 10 Mbps |
| Maximum Cable Length | 4000 ft. | 4000 ft. |
| Minimum Driver Output Voltage | $\pm 2\text{ V}$ | $\pm 1.5\text{ V}$ |
| Driver Load Impedance | $100\ \Omega$ | $54\ \Omega$ |
| Receiver Input Resistance | $4\text{ k}\Omega$ minimum | $12\text{ k}\Omega$ minimum |
| Receiver Input Sensitivity | $\pm 200\text{ mV}$ | $\pm 200\text{ mV}$ |
| Receiver Input Voltage Range | -7 V to $+7\text{ V}$ | -7 V to $+12\text{ V}$ |
| Number of Drivers/Receivers per Line | 1/10 | 32/32 |

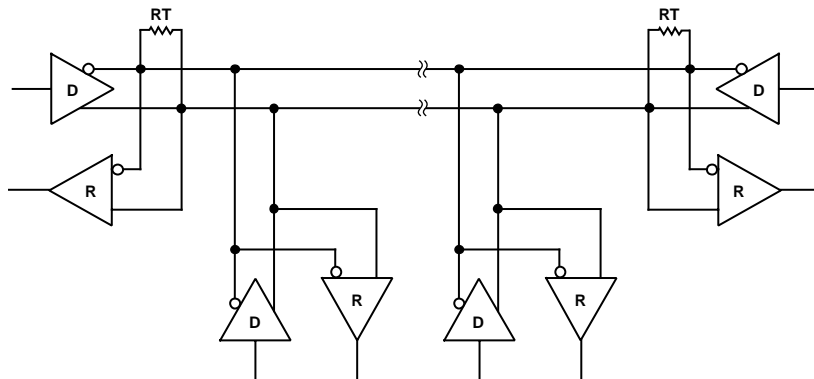
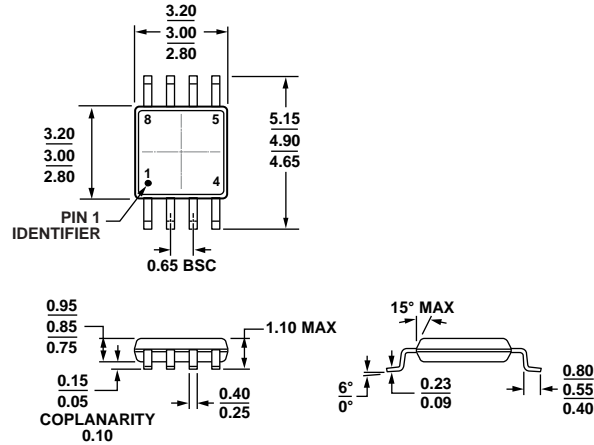


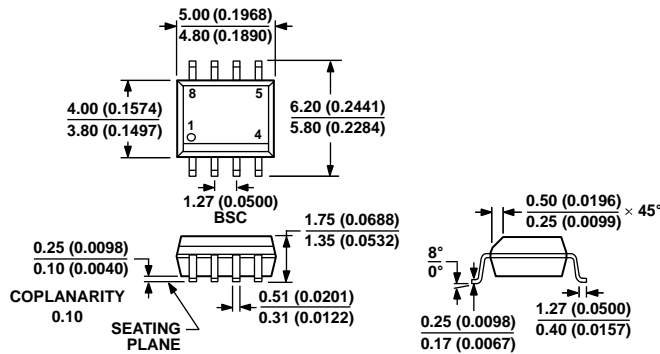
Figure 22. Typical RS-485 Network

09488-022

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA
 Figure 23. 8-Lead Mini Small Outline Package [MSOP]
 (RM-8)
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 Figure 24. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 25. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

Dimensions shown in millimeters

001708-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

060608-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding |
|--------------------|-------------------|--|----------------|----------|
| ADM488ABRMZ | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | FOF |
| ADM488ABRMZ-REEL7 | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | FOF |
| ADM488ABRZ | -40°C to +85°C | 8-Lead Standard Small Outline Package, Narrow Body [SOIC_N] | R-8 | |
| ADM488ABRZ-REEL7 | -40°C to +85°C | 8-Lead Standard Small Outline Package, Narrow Body [SOIC_N] | R-8 | |
| ADM489ABRMZ | -40°C to +85°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | FOG |
| ADM489ABRMZ-REEL7 | -40°C to +85°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | FOG |
| ADM489ABRZ | -40°C to +85°C | 14-Lead Standard Small Outline Package, Narrow Body [SOIC_N] | R-14 | |
| ADM489ABRZ-REEL7 | -40°C to +85°C | 14-Lead Standard Small Outline Package, Narrow Body [SOIC_N] | R-14 | |

¹ Z = RoHS Compliant Part.

NOTES