

# DDR4 SDRAM SODIMM Addendum

## MTA18ASF2G72HBZ – 16GB

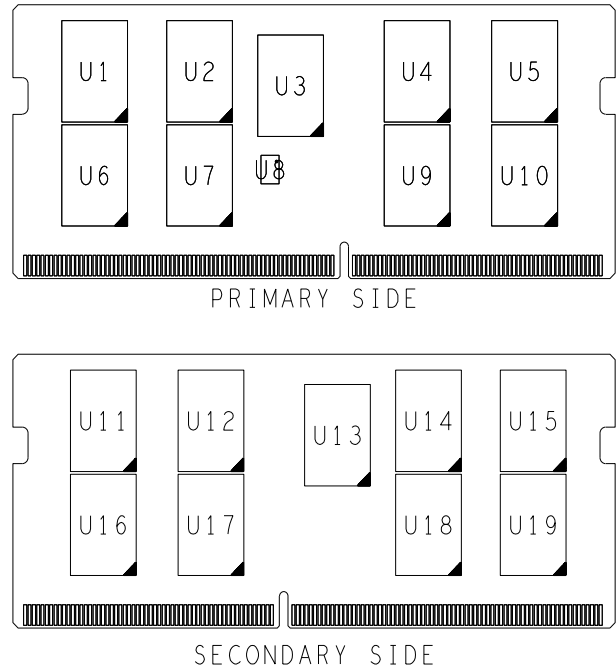
### Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 SODIMM Core data sheet.

### Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 SODIMM Core data sheet
- 260-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rate: PC4-3200
- 16GB (2 Gig x 72)
- Data bus inversion (DBI) for data bus
- Supports ECC error detection and correction
- Dual-rank
- Onboard I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 260-Pin SODIMM



### Options

- Operating temperature
  - Extended ( $-40^{\circ}\text{C} \leq T_{\text{OPER}} \leq 105^{\circ}\text{C}$ )
- Package
  - 260-pin DIMM (Green)
- Frequency/CAS latency
  - 0.625ns @ CL = 22 (DDR4-3200)

### Marking

B  
Z  
-3G2

Table 1: Addressing

Parameter	16GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	CS_n[1:0]



**Table 2: Part Numbers and Timing Parameters – 16GB Modules**

Base device: MT40A1G8,<sup>1</sup> 8Gb DDR4 SDRAM

<b>Part Number<sup>2</sup></b>	<b>Module Density</b>	<b>Configuration</b>	<b>Module Bandwidth</b>	<b>Memory Clock/ Data Rate</b>	<b>Clock Cycles (CL-nRCD-nRP)</b>
MTA18ASF2G72HBZ-3G2__	16GB	2 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22

- Notes:
1. The data sheet for the base device can be found on Micron’s web site.
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA18ASF2G72HBZ-3G2E1.

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## DQ Maps

Table 3: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	11	42	U2	0	27	84
	1	8	28		1	25	71
	2	10	41		2	26	83
	3	9	29		3	24	70
	4	14	38		4	31	80
	5	12	24		5	29	67
	6	15	37		6	30	79
	7	13	25		7	28	66
U3	0	CB3	105	U4	0	34	187
	1	CB0	92		1	33	173
	2	CB2	101		2	35	186
	3	CB1	91		3	32	174
	4	CB6	100		4	39	182
	5	CB4	88		5	36	170
	6	CB7	104		6	38	183
	7	CB5	87		7	37	169
U5	0	51	229	U6	0	2	20
	1	49	215		1	0	8
	2	50	228		2	3	21
	3	48	216		3	1	7
	4	55	225		4	6	16
	5	53	212		5	4	4
	6	54	224		6	7	17
	7	52	211		7	5	3
U7	0	22	58	U9	0	42	207
	1	20	46		1	40	195
	2	23	59		2	43	208
	3	21	45		3	41	194
	4	18	62		4	46	203
	5	16	50		5	45	190
	6	19	63		6	47	204
	7	17	49		7	44	191

**Table 3: Component-to-Module DQ Map, Front (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	59	250				
	1	57	236				
	2	58	249				
	3	56	237				
	4	63	246				
	5	61	233				
	6	62	245				
	7	60	232				

**Table 4: Component-to-Module DQ Map, Back**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	49	215	U12	0	33	173
	1	51	229		1	34	187
	2	48	216		2	32	174
	3	50	228		3	35	186
	4	53	212		4	36	170
	5	55	225		5	39	182
	6	52	211		6	37	169
	7	54	224		7	38	183
U13	0	CB0	92	U14	0	25	71
	1	CB3	105		1	27	84
	2	CB1	91		2	24	70
	3	CB2	101		3	26	83
	4	CB4	88		4	29	67
	5	CB6	100		5	31	80
	6	CB5	87		6	28	66
	7	CB7	104		7	30	79



**Table 4: Component-to-Module DQ Map, Back (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U15	0	8	28	U16	0	57	236
	1	11	42		1	59	250
	2	9	29		2	56	237
	3	10	41		3	58	249
	4	12	24		4	61	233
	5	14	38		5	63	246
	6	13	25		6	60	232
	7	15	37		7	62	245
U17	0	40	195	U18	0	20	46
	1	42	207		1	22	58
	2	41	194		2	21	45
	3	43	208		3	23	59
	4	45	190		4	16	50
	5	46	203		5	18	62
	6	44	191		6	17	49
	7	47	204		7	19	63
U19	0	0	8				
	1	2	20				
	2	1	7				
	3	3	21				
	4	4	4				
	5	6	16				
	6	5	3				
	7	7	17				

## I<sub>DD</sub> Specifications

**Table 5: DDR4 I<sub>DD</sub> Specifications and Conditions – 16GB (Die Revision E)**

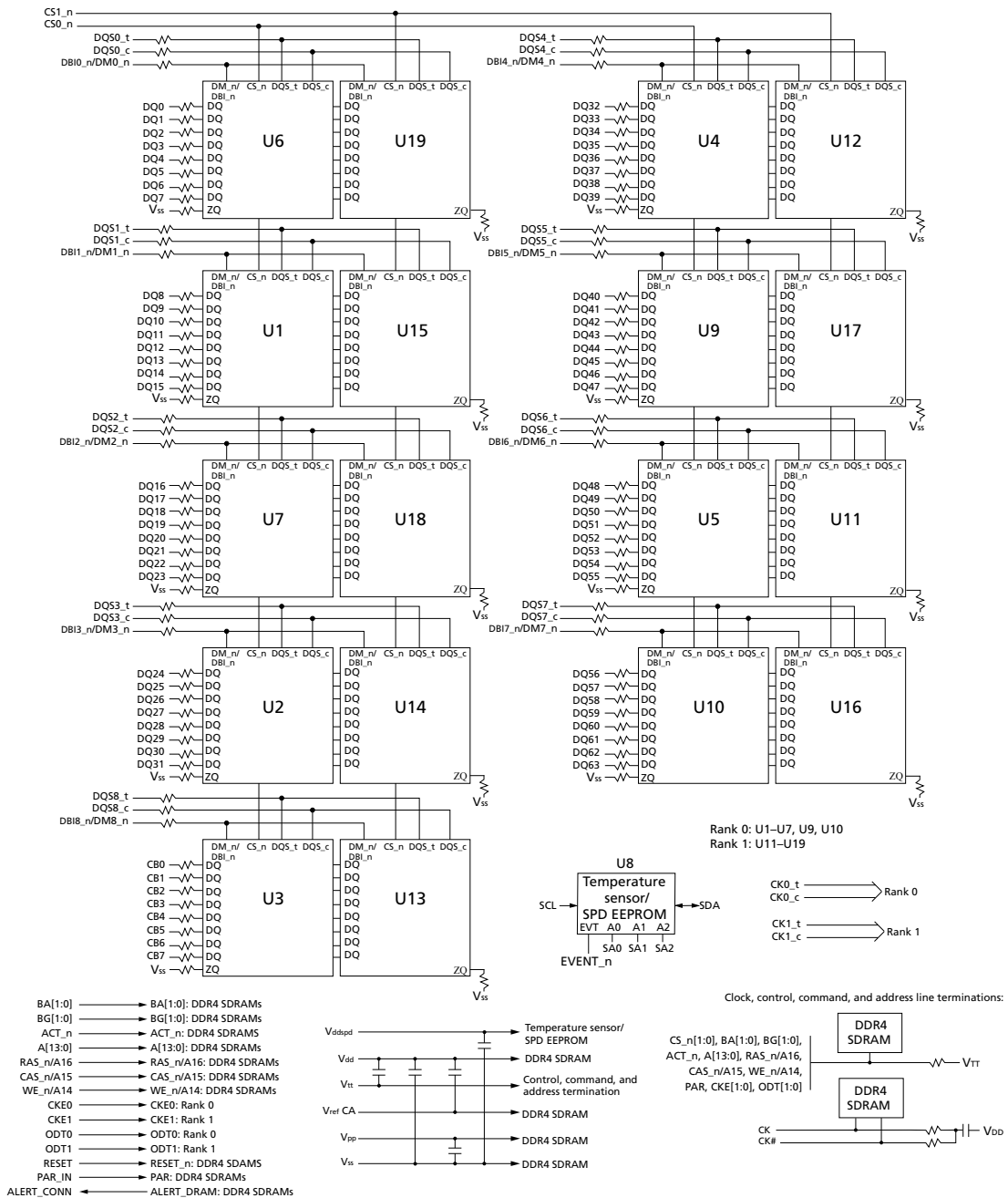
Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub> <sup>1</sup>	693	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, IPP current	I <sub>PP0</sub> <sup>1</sup>	54	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>DD1</sub> <sup>1</sup>	837	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	648	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	666	mA
Precharge power-down current	I <sub>DD2P</sub> <sup>2</sup>	468	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	522	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	846	mA
Active standby I <sub>pp</sub> current	I <sub>PP3N</sub> <sup>2</sup>	54	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	666	mA
Burst read current	I <sub>DD4R</sub> <sup>1</sup>	1935	mA
Burst write current	I <sub>DD4W</sub> <sup>1</sup>	1674	mA
Burst refresh current (1x REF)	I <sub>DD5R</sub> <sup>1</sup>	1134	mA
Burst refresh I <sub>pp</sub> current (1x REF)	I <sub>PP5R</sub> <sup>1</sup>	72	mA
Self refresh current: Normal temp range (0–85°C)	I <sub>DD6N (0–85°C)</sub> <sup>2</sup>	612	mA
Self refresh current: Extended temp range (0–95°C)	I <sub>DD6E (0–95°C)</sub> <sup>2</sup>	1710	mA
Self refresh current: Reduced temp range (0–45°C)	I <sub>DD6R (0–45°C)</sub> <sup>2</sup>	378	mA
Auto self refresh current (25°C)	I <sub>DD6A (25°C)</sub> <sup>2</sup>	155	mA
Auto self refresh current (45°C)	I <sub>DD6A (45°C)</sub> <sup>2</sup>	378	mA
Auto self refresh current (75°C)	I <sub>DD6A (75°C)</sub> <sup>2</sup>	558	mA
Auto self refresh current (95°C)	I <sub>DD6A (95°C)</sub> <sup>2</sup>	1710	mA
Auto self refresh I <sub>pp</sub> current	I <sub>PP6X</sub> <sup>2</sup>	108	mA
Bank interleave read current	I <sub>DD7</sub> <sup>1</sup>	1989	mA
Bank interleave read IPP current	I <sub>PP7</sub> <sup>1</sup>	144	mA
Maximum Power Down Current	I <sub>DD8</sub> <sup>2</sup>	360	mA

- Notes: 1. One module rank in the active I<sub>DD/PP</sub>, the other rank in I<sub>DD2P/PP3N</sub>.  
2. All ranks in this I<sub>DD/PP</sub> condition.

## Functional Block Diagrams

Figure 2: Functional Block Diagram

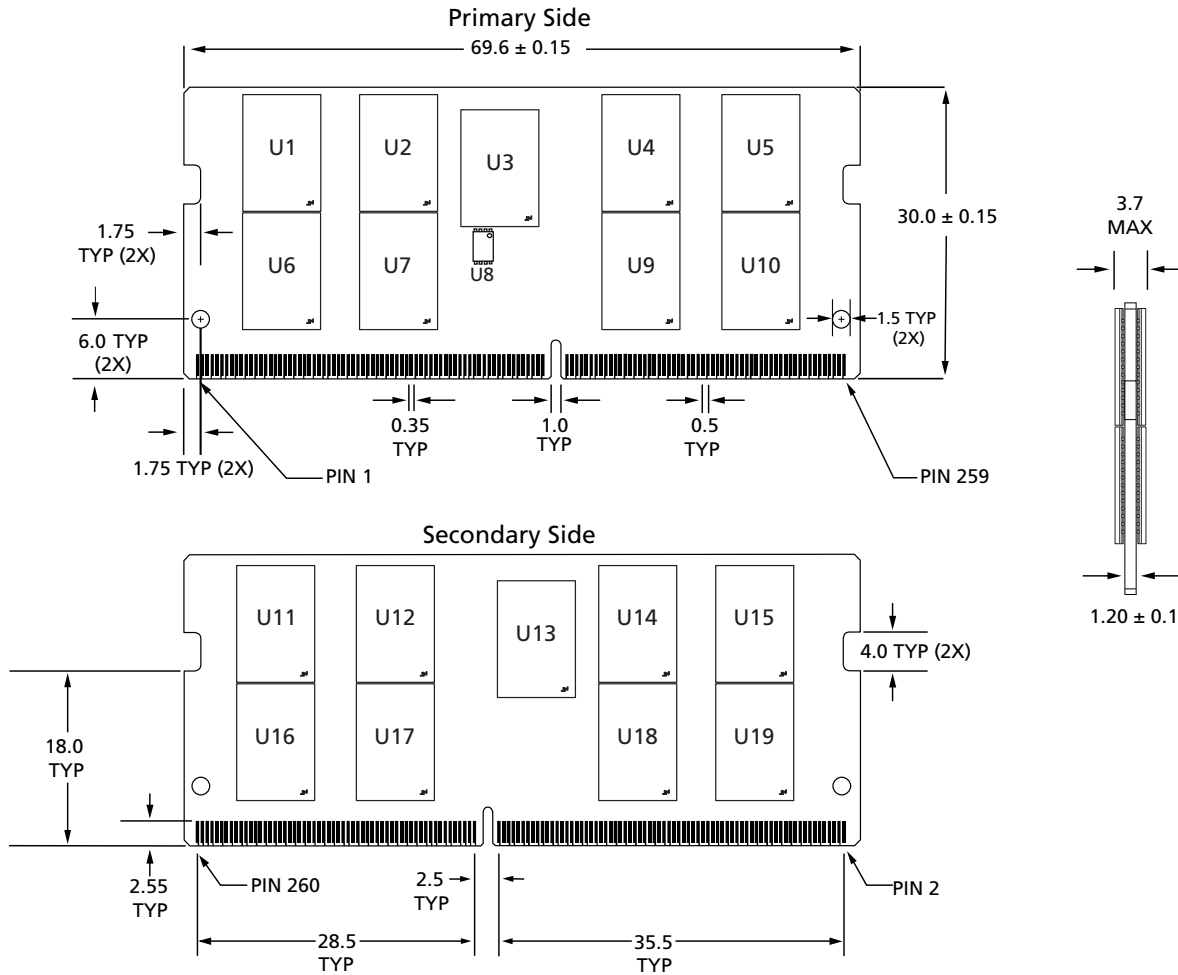


Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



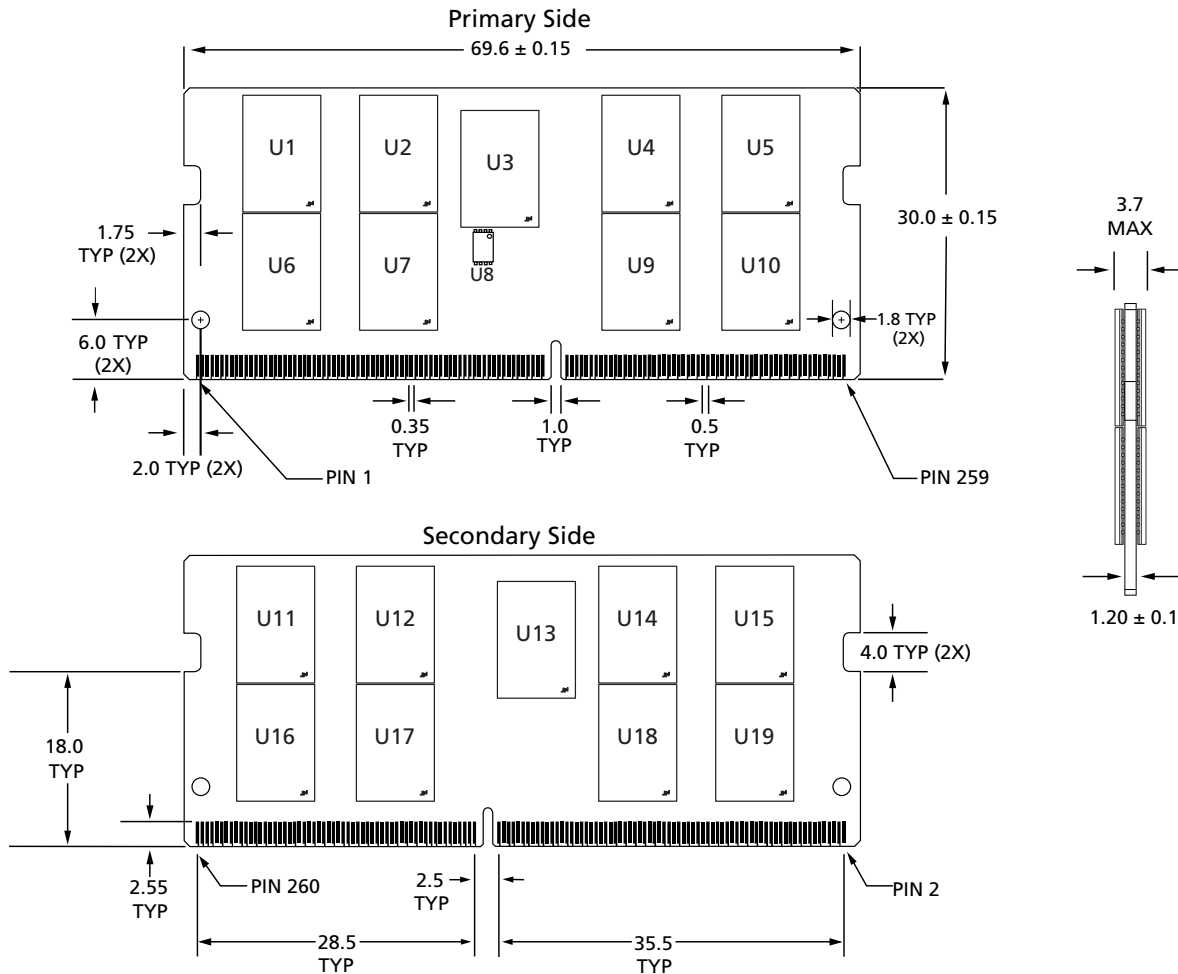
## Module Dimensions

Figure 3: 260-Pin DDR4 SODIMM - PCB 2975



- Notes:
1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
  2. Tolerance on all dimensions  $\pm 0.15$ mm unless otherwise specified.
  3. The dimensional diagram is for reference only.

**Figure 4: 260-Pin DDR4 SODIMM - PCB 3218**



- Notes:
1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
  2. Tolerance on all dimensions  $\pm 0.15$ mm unless otherwise specified.
  3. The dimensional diagram is for reference only.

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